

## Concurrent Error Detection, Diagnosis, and Fault Tolerance for Switched-Capacitor Filters

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In this paper, a concurrent error detection, diagnosis, and fault tolerance methodology for switched-capacitor filters (SCFs) based on the checksum code method is presented. By adding one and two rows to the state equation matrices of an SCF, concurrent error detection and diagnosis schemes can be respectively developed. The fault tolerance scheme can be obtained by feeding back the error detection results to the original circuit. We show that the area overhead of the concurrent error detection circuit can be significantly reduced by simplifying the derived switched-capacitor test circuits. A fifth order low-pass Chebyshev filter has been designed to verify the proposed schemes. Simulation results validate the effectiveness of this method.

**Keywords:** analog circuit testing, concurrent testing, error detection, fault diagnosis, fault tolerance, switched-capacitor filters.

### 1. INTRODUCTION

The switched-capacitor filter (SCF) technique offers an attractive solution to the design of active filters [1]. This is because in the SCF technique large amounts of resistance can be easily emulated by the combination of small value capacitors and MOS switching transistors; hence, the entire active filter circuit can be easily implemented in a single IC chip. In addition, the time constant of a switched-capacitor filter is quite precise and easy to control because it depends on a ratio of capacitors which can be adjusted via the sampling frequency. Unfortunately, similar to many other single chip designs, the testing problem for these circuits is quite difficult due to the fact that the accessible lines of a circuit under test (CUT) are limited to the I/O pins of the chip.

Various design for testability (DFT) techniques to enhance circuit controllability and observability for digital circuits have been widely used [2]. These techniques are difficult to apply to analog circuits due to the intrinsic difference between digital and analog circuits. In the digital domain only 0 and 1 are concerned, while in the analog domain, a circuit usually functions within a specified range. As a result, the later is, in general, much more difficult to apply than the former.

To our knowledge there exist very few papers on switched-capacitor circuit

testing. In [3], an architecture that can perform off- and on-line tests for SCFs is proposed. This approach uses a programmable biquad to provide a comparison (voting) mechanism for each stage of a filter. Whether or not the programmable biquad and the biquads of a filter element have a similar response during their actual operations indicates the correctness of the element. Unfortunately, it is difficult to design a programmable biquad with high precision and low hardware overhead. In [4], a DFT methodology to improve the controllability and observability of internal signals in SC circuits is presented. This methodology may alter the structure of original circuits and, hence, may greatly affect the circuit performance.

In this paper, we propose a concurrent error detection, diagnosis, and correction scheme that can be applied to SCFs. The concurrent error detection scheme makes possible the monitoring of an SCF during its normal operation, the diagnosis scheme allows one to identify the faulty site down to the single SC stage level, while the fault tolerance scheme can greatly reduce the fault effect during its normal operation and thus, can significantly increase the reliability of an SCF circuit.

Our work is similar to that presented by Chatterjee in [5-7]: both are based on the checksum code technique and the test circuits for error detection, fault diagnosis, and fault tolerance are derived by augmenting the state equation of analog circuits. However, the work presented here differs from [5-7] in the following aspects. First, we deal with discrete-time circuits such as SCFs while in [5-7] the main focus is on continuous-time analog circuits. Second, we analyze the circuits directly in the  $z$ -domain instead of the  $s$ -domain. This allows us to deal with SCFs that have already been designed without converting them back to their RC filter counterpart as suggested in [5]. Third, we present some simplification rules to simplify the test circuits so as to reduce the area overhead. This is especially useful for SCFs circuits.

The organization of this paper is as follows. In Section 2, some background on SCFs is reviewed which includes the building blocks of SCFs and the formulation of state equations for SCFs in  $z$ -domain. In Section 3, concurrent error detection methodology for SCFs is detailed. Relation between a fault and the error indication is also described. In Section 4, fault diagnosis methodology and hardware architecture are described. The fault tolerance scheme is presented in Section 5. The simplification rules of test circuitry are presented in Section 6. A fifth-order, low-pass Chebyshev filter has been designed and simulation results are presented in Section 7. Finally in Section 8 we summarize the presented work and suggest some future directions for research.

## 2. BASIS OF SWITCHED-CAPACITOR FILTERS

In this section, some necessary background about switched-capacitor filters is provided. One may refer to [8, 9] for more information about these filters. Most switched-capacitor filter structures have resulted from the substitution of an active-RC filter's continuous-time integrators by their switched-capacitor counterparts. This approach has been applied to biquads as well as LC ladder filters. Three of the principal switched-capacitor integrator building blocks are shown in Fig. 1 [8, 10].

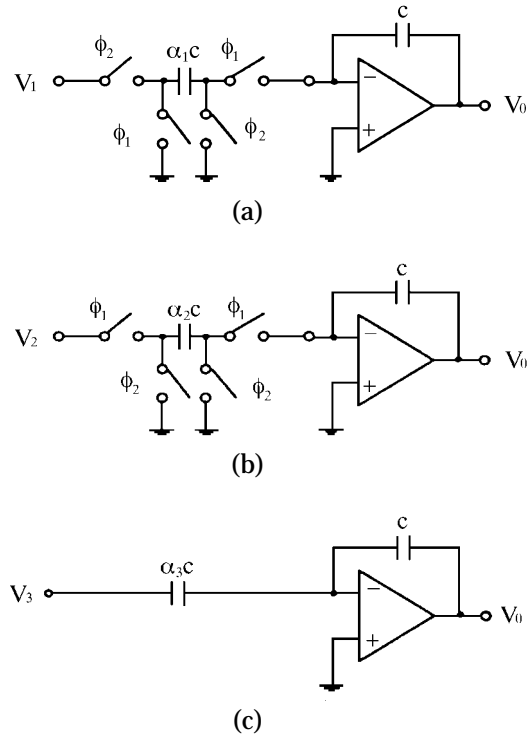


Fig. 1. Switched-capacitor circuits. (a) non-inverting lossless integrator, (b) inverting lossless integrator, and (c) inverting feed-forward integrator.

The non-inverting SC integrator (Fig. 1(a)) operates as follows. During phase  $\phi_2$  of the non-overlapping clock period  $(n - 1)$ , the charge on capacitor  $C$  holds the output voltage  $V_o(n - 1)$ , while capacitor  $\alpha_1 C$  is charged to  $V_1(n - 1)$ . During the next clock phase, i.e.,  $\phi_1$  of period  $(n)$ , capacitor  $\alpha_1 C$  is discharged into capacitor  $C$  causing the output voltage to charge to  $V_o(n)$ . It is easy to show that  $V_o(n) = V_o(n - 1) + \alpha_1 V_1(n - 1)$ , which gives the  $z$ -domain transfer function  $H_1(z) = \frac{V_o(z)}{V_1(z)} = \frac{\alpha_1 z^{-1}}{1 - z^{-1}}$ .

The inverting SC integrator shown in Fig. 1(b) operates similarly. During clock phase  $\phi_2$  of period  $(n - 1)$ , capacitor  $C$  holds the output voltage at  $V_o(n - 1)$  while capacitor  $\alpha_2 C$  is discharged. During the next  $\phi_1$  clock phase of period  $(n)$ , capacitor  $\alpha_2 C$  is charged to  $V_2(n)$  and capacitor  $C$  charged to  $V_o(n)$ . It is also easy to show that  $V_o(n) = V_o(n - 1) - \alpha_2 V_2(n)$  and the transfer function is  $H_2(z) = \frac{V_o(z)}{V_2(z)} = -\frac{\alpha_2}{1 - z^{-1}}$ .

The inverting feed-forward integrator shown in Fig. 1(c) operates as follows. At time  $(n - 1)$ , capacitor  $C$  holds the output voltage  $V_o(n - 1)$  and capacitor  $\alpha_3 C$  is charged to  $V_3(n - 1)$ . At time  $(n)$ , capacitor  $\alpha_3 C$  is charged to  $V_3(n)$  and transfers a total charge of magnitude  $(V_3(n) - V_3(n - 1))\alpha_3 C$  into capacitor  $C$  causing the output voltage to charge to  $V_o(n)$ . Thus  $V_o(n) = V_o(n - 1) - \alpha_3(V_3(n) - V_3(n - 1))$

and the transfer function is  $H_3(z) = \frac{V_o(z)}{V_3(z)} = -\alpha_3$ . Note that an inverting feed-forward integrator can be replaced by a non-inverting and inverting integrators because  $H_3(z) = -\alpha_3$  can be divided into  $\frac{\alpha_3 z^{-1}}{1-z^{-1}}$  and  $\frac{-\alpha_3}{1-z^{-1}}$ .

In this paper, we shall concentrate on switched-capacitor filters composed of the three types of integrators discussed above. The same concept can be applied to other discrete-time circuits with similar state equations. We represent the output of the  $i$ 'th integrator as a state variable  $x_i(z)$ . Thus a circuit with  $n$  integrators can be represented as a matrix called a state vector  $[x_1(z), x_2(z), \dots, x_n(z)]^T$ . Let  $u(z)$  be the input of the circuit, then the state equation of the circuit can be described by  $\mathbf{X}(z) = \mathbf{A}(z)\mathbf{X}(z) + \mathbf{B}(z)u(z)$  where  $\mathbf{A}(z)$ ,  $\mathbf{X}(z)$ ,  $\mathbf{B}(z)$  are  $n \times n$ ,  $n \times 1$ , and  $n \times 1$  matrices, respectively. Because we assume that a filter is composed of integrators, the relation between the input and the output of integrators in a filter may be represented as  $\frac{a}{1-z^{-1}}$ ,  $\frac{bz^{-1}}{1-z^{-1}}$  or  $\frac{a+bz^{-1}}{1-z^{-1}}$ . The state equation can therefore be expanded as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ \vdots \\ x_n(z) \end{bmatrix} = \begin{bmatrix} \frac{a_{11} + b_{11}z^{-1}}{1-z^{-1}} & \cdots & \frac{a_{1n} + b_{1n}z^{-1}}{1-z^{-1}} \\ \frac{a_{21} + b_{21}z^{-1}}{1-z^{-1}} & \cdots & \frac{a_{2n} + b_{2n}z^{-1}}{1-z^{-1}} \\ \vdots & \ddots & \vdots \\ \frac{a_{n1} + b_{n1}z^{-1}}{1-z^{-1}} & \cdots & \frac{a_{nn} + b_{nn}z^{-1}}{1-z^{-1}} \end{bmatrix} \begin{bmatrix} x_1(z) \\ x_2(z) \\ \vdots \\ x_n(z) \end{bmatrix} + \begin{bmatrix} \frac{c_1 + d_1z^{-1}}{1-z^{-1}} \\ \frac{c_2 + d_2z^{-1}}{1-z^{-1}} \\ \vdots \\ \frac{c_n + d_nz^{-1}}{1-z^{-1}} \end{bmatrix} u(z)$$

$$= \begin{bmatrix} a_{11} + b_{11}z^{-1} & \cdots & a_{1n} + b_{1n}z^{-1} \\ a_{21} + b_{21}z^{-1} & \cdots & a_{2n} + b_{2n}z^{-1} \\ \vdots & \ddots & \vdots \\ a_{n1} + b_{n1}z^{-1} & \cdots & a_{nn} + b_{nn}z^{-1} \end{bmatrix} \begin{bmatrix} \frac{x_1(z)}{1-z^{-1}} \\ \frac{x_2(z)}{1-z^{-1}} \\ \vdots \\ \frac{x_n(z)}{1-z^{-1}} \end{bmatrix} + \begin{bmatrix} c_1 + d_1z^{-1} \\ c_2 + d_2z^{-1} \\ \vdots \\ c_n + d_nz^{-1} \end{bmatrix} \frac{u(z)}{1-z^{-1}}$$

or  $\mathbf{X}(z) = \mathbf{A}'(z)\frac{\mathbf{X}(z)}{1-z^{-1}} + \mathbf{B}'(z)\frac{u(z)}{1-z^{-1}}$ . The coefficients  $a_{ij}$ ,  $b_{ij}$ ,  $c_i$  and  $d_i$  for  $1 \leq i, j \leq n$ , in matrices  $\mathbf{A}(z)$  and  $\mathbf{B}(z)$  are obtained according to the relation of any two state variables and the relation between  $x_i(z)$  and  $u(z)$ . In fact, they represent various capacitance ratios in the filters.

For example, Fig. 2(a) shows a biquadratic filter (biquad) [11] and Fig. 2(b) shows its signal flow graph. Assume the outputs of  $OA_1$  and  $OA_2$  are  $x_1$  and  $x_2$ , respectively. The matrices  $\mathbf{A}'(z)$  and  $\mathbf{B}'(z)$  can be represented as

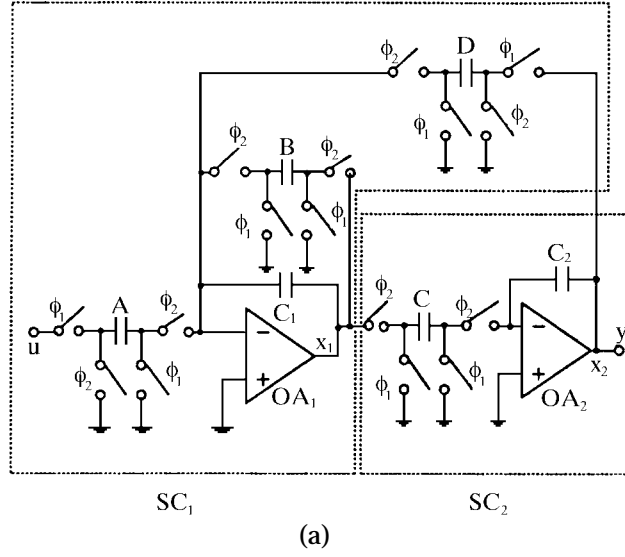


Fig. 2. (a) A biquadratic filter and (b) its SFG.

$\mathbf{A}'(z) = \begin{bmatrix} -\frac{B}{C_1} & \frac{D}{C_1}z^{-1} \\ -\frac{C}{C_2} & 0 \end{bmatrix}$  and  $\mathbf{B}'(z) = \begin{bmatrix} \frac{A}{C_1}z^{-1} \\ 0 \end{bmatrix}$ . The state equation of Fig. 2 can be represented as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \end{bmatrix} = \begin{bmatrix} -\frac{B}{C_1} & \frac{D}{C_1}z^{-1} \\ -\frac{C}{C_2} & 0 \end{bmatrix} \begin{bmatrix} \frac{x_1(z)}{1-z^{-1}} \\ \frac{x_2(z)}{1-z^{-1}} \end{bmatrix} + \begin{bmatrix} \frac{A}{C_1}z^{-1} \\ 0 \end{bmatrix} \frac{u(z)}{1-z^{-1}} \quad (1)$$

### 3. CONCURRENT ERROR DETECTION METHODOLOGY

#### 3.1 Formulation

Consider an  $(n + 1) \times (n + 1)$  matrix  $\mathbf{A}''(z) = \begin{bmatrix} \mathbf{A}'(z) & 0 \\ \mathbf{A}_1(z) & 0 \end{bmatrix}$  where  $\mathbf{A}_1(z)$  is a  $1 \times n$  matrix and  $\mathbf{A}_1(z) = [\gamma_1(z), \gamma_2(z), \dots, \gamma_n(z)] = [\alpha_1, \alpha_2, \dots, \alpha_n] \cdot \mathbf{A}'(z)$ . The vector  $[\alpha_1, \alpha_2, \dots, \alpha_n]$ , called a *coding vector* (C.V.), is a vector of arbitrary real numbers. The rightmost column of  $\mathbf{A}''(z)$  is the zero column. For  $\mathbf{B}'(z)$ , we derive an  $(n + 1) \times 1$  matrix  $\mathbf{B}''(z)$  such that  $\mathbf{B}''(z) = \begin{bmatrix} \mathbf{B}'(z) \\ \beta(z) \end{bmatrix}$  where  $\beta(z) = [\alpha_1, \alpha_2, \dots, \alpha_n] \cdot \mathbf{B}'(z)$ . The modified matrix  $\mathbf{A}''(z)$  and  $\mathbf{B}''(z)$  can be used to form a modified state equation  $\mathbf{X}''(z) = \mathbf{A}''(z) \frac{\mathbf{X}''(z)}{1 - z^{-1}} + \mathbf{B}''(z) \frac{u(z)}{1 - z^{-1}}$  where the state vector  $\mathbf{X}''(z) = [x_1(z), x_2(z), \dots, x_n(z), x_{n+1}(z)]^T$ . This modified state equation can be expanded as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ \vdots \\ x_n(z) \\ x_{n+1}(z) \end{bmatrix} = \begin{bmatrix} a_{11} + b_{11}z^{-1} & \cdots & a_{1n} + b_{1n}z^{-1} & 0 \\ a_{21} + b_{21}z^{-1} & \cdots & a_{2n} + b_{2n}z^{-1} & 0 \\ \vdots & \ddots & \vdots & \vdots \\ a_{n1} + b_{n1}z^{-1} & \cdots & a_{nn} + b_{nn}z^{-1} & 0 \\ \gamma_1(z) & \cdots & \gamma_n(z) & 0 \end{bmatrix} \begin{bmatrix} \frac{x_1(z)}{1 - z^{-1}} \\ \frac{x_2(z)}{1 - z^{-1}} \\ \vdots \\ \frac{x_n(z)}{1 - z^{-1}} \\ \frac{x_{n+1}(z)}{1 - z^{-1}} \end{bmatrix} + \begin{bmatrix} c_1 + d_1z^{-1} \\ c_2 + d_2z^{-1} \\ \vdots \\ c_n + d_nz^{-1} \\ \beta(z) \end{bmatrix} \frac{u(z)}{1 - z^{-1}} \quad (2)$$

The additional state variable  $x_{n+1}(z)$  is used to construct the test circuitry. Next we present the theoretical basis of the fault detection circuitry.

**Theorem 1:** In the modified state equation  $\mathbf{X}''(z) = \mathbf{A}''(z) \frac{\mathbf{X}''(z)}{1 - z^{-1}} + \mathbf{B}''(z) \frac{u(z)}{1 - z^{-1}}$ ,  $x_{n+1}(z) = \sum_{i=1}^n \alpha_i x_i(z)$ .

**Proof:** According to the modified state equation (Eq. (2)), we have

$$x_{n+1}(z) = \gamma_1(z) \frac{x_1(z)}{1 - z^{-1}} + \gamma_2(z) \frac{x_2(z)}{1 - z^{-1}} + \cdots + \gamma_n(z) \frac{x_n(z)}{1 - z^{-1}} + \beta(z) \frac{u(z)}{1 - z^{-1}} \quad (3)$$

From the definition of  $\gamma_1(z)$ ,  $\gamma_2(z)$ , ...,  $\gamma_n(z)$  and  $\beta(z)$ , we get the following equations:

$$\begin{aligned}\gamma_1(z) &= [\alpha_1, \dots, \alpha_n][a_{11} + b_{11}z^{-1}, \dots, a_{n1} + b_{n1}z^{-1}]^T \\ &= \alpha_1(a_{11} + b_{11}z^{-1}) + \dots + \alpha_n(a_{n1} + b_{n1}z^{-1})\end{aligned}$$

⋮

$$\begin{aligned}\gamma_n(z) &= [\alpha_1, \dots, \alpha_n][a_{1n} + b_{1n}z^{-1}, \dots, a_{nn} + b_{nn}z^{-1}]^T \\ &= \alpha_1(a_{1n} + b_{1n}z^{-1}) + \dots + \alpha_n(a_{nn} + b_{nn}z^{-1})\end{aligned}$$

$$\begin{aligned}\beta(z) &= [\alpha_1, \dots, \alpha_n][c_1 + d_1z^{-1}, \dots, c_n + d_nz^{-1}]^T \\ &= \alpha_1(c_1 + d_1z^{-1}) + \dots + \alpha_n(c_n + d_nz^{-1})\end{aligned}$$

Substituting these equations into Eq. (3), we have

$$\begin{aligned}x_{n+1}(z) &= [\alpha_1(a_{11} + b_{11}z^{-1}) + \dots + \alpha_n(a_{n1} + b_{n1}z^{-1})] \frac{x_1(z)}{1 - z^{-1}} \\ &\quad + \dots \\ &\quad + [\alpha_1(a_{1n} + b_{1n}z^{-1}) + \dots + \alpha_n(a_{nn} + b_{nn}z^{-1})] \frac{x_n(z)}{1 - z^{-1}} \\ &\quad + [\alpha_1(c_1 + d_1z^{-1}) + \dots + \alpha_n(c_n + d_nz^{-1})] \frac{u(z)}{1 - z^{-1}} \\ &= \alpha_1 x_1(z) + \dots + \alpha_n x_n(z) \\ &= \sum_{i=1}^n \alpha_i x_i(z)\end{aligned}$$

This proves the Theorem. □

**Corollary 1:** In the modified state equation  $\mathbf{X}''(z) = \mathbf{A}''(z) \frac{\mathbf{X}''(z)}{1 - z^{-1}} + \mathbf{B}''(z) \frac{u(z)}{1 - z^{-1}}$ ,  
 $\sum_{i=1}^n \alpha_i x_i(z) = \sum_{i=1}^n \gamma_i(z) \frac{x_i(z)}{1 - z^{-1}} + \beta(z) \frac{u(z)}{1 - z^{-1}}$ .

**Proof:** Follows directly from Eq. (3) and Theorem 1. □

According to Corollary 1, a concurrent error detection (CED) scheme can be developed. This is best explained using the signal flow graph (SFG) representation. Fig. 3 is the signal flow graph of the concurrent error detection scheme. In this

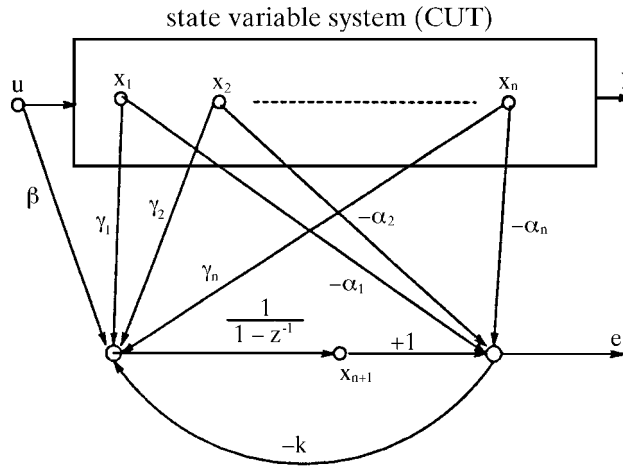


Fig. 3. SFG of CED scheme.

figure, we define the error line as  $e(z) = \sum_{i=1}^n \gamma_i(z) \frac{x_i(z)}{1-z^{-1}} + \beta(z) \frac{u(z)}{1-z^{-1}} - \sum_{i=1}^n \alpha_i x_i(z)$ .

According to Corollary 1,  $e(z)$  is zero if there is no fault in the CUT. In the following subsection we shall show that if there exists a fault in the circuit that causes the representation of some state variable  $x_i(z)$  to differ from its normal representation, then  $e(z)$  must become nonzero. Thus by monitoring  $e(z)$ , the fault can be detected. In fact, not only can a fault in CUT be detected by the test circuit but also a fault in the test circuit can be detected by itself.

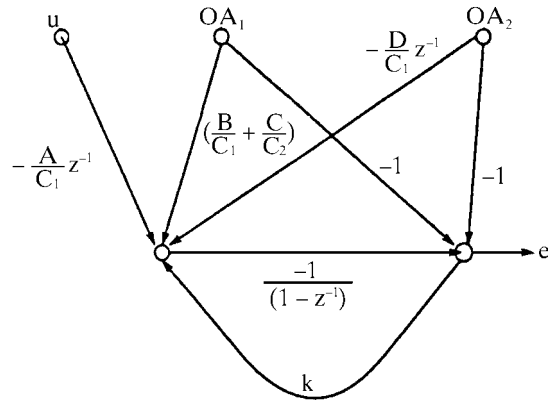
Note that the test circuit may be unstable due to a pole of the integrator at  $z = 1$  in  $z$ -domain (which corresponds to  $s = 0$  in  $s$ -domain as  $z = e^{sT}$ ). Thus the negative feedback with gain  $k$  in Fig. 3 is necessary to stabilize the test circuit.

As an example, assume the coding vector =  $[1, 1]$  for Fig. 2, then the modified state equation is

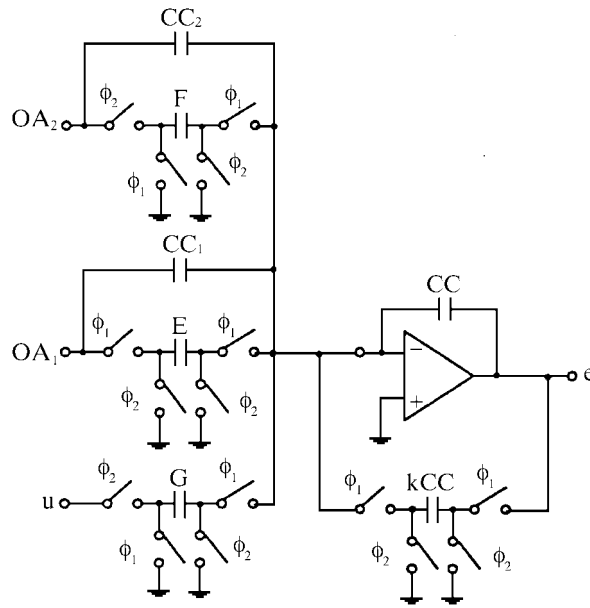
$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ x_3(z) \end{bmatrix} = \begin{bmatrix} -\frac{B}{C_1} & \frac{D}{C_1}z^{-1} & 0 \\ -\frac{C}{C_2} & 0 & 0 \\ -(\frac{B}{C_1} + \frac{C}{C_2}) & \frac{D}{C_1}z^{-1} & 0 \end{bmatrix} \begin{bmatrix} \frac{x_1(z)}{1-z^{-1}} \\ \frac{x_2(z)}{1-z^{-1}} \\ \frac{x_3(z)}{1-z^{-1}} \end{bmatrix} + \begin{bmatrix} \frac{A}{C_1}z^{-1} \\ 0 \\ \frac{A}{C_1}z^{-1} \end{bmatrix} \frac{u(z)}{1-z^{-1}}$$

Fig. 4(a) is the signal flow graph of the test circuit and Fig. 4(b) is its hardware realization. Note that in Fig. 4 we set  $\frac{CC_2}{CC} = \frac{CC_1}{CC} = 1$ ,  $\frac{E}{CC} = \frac{B}{C_1} + \frac{C}{C_2}$ ,  $\frac{F}{CC} = \frac{D}{C_1}$ , and  $\frac{G}{CC} = \frac{A}{C_1}$ .

Let the values of the capacitors  $A, B, C$  and  $D$  be 0.1pF,  $C_1$  and  $C_2$  be 2pF,  $CC_1 = CC_2 = CC = 2pF$ ,  $E = B + C = 0.2pF$ ,  $F = D = 0.1pF$ ,  $G = A = 0.1pF$ , and  $k = 0.1$ . The circuit is simulated by SWITCAP (a switched-capacitor circuit



(a)



(b)

Fig. 4. (a) SFG of the test circuit for the biquadratic filter and (b) its hardware implementation.

simulator). The responses of the CUT (low-pass and bandpass filter) and the error line ( $e(z)$ ) under fault free conditions are shown in Fig. 5(a). As expected, the error line is almost zero for all frequencies in fault-free conditions. When capacitor  $A$  is changed to 0.15pF, the responses of the low-pass, bandpass, and error line are shown in Fig. 5(b). The magnitudes of the passbands of both the low-pass and bandpass are changed to about 1.5V and the magnitude of the error line becomes much greater than zero.

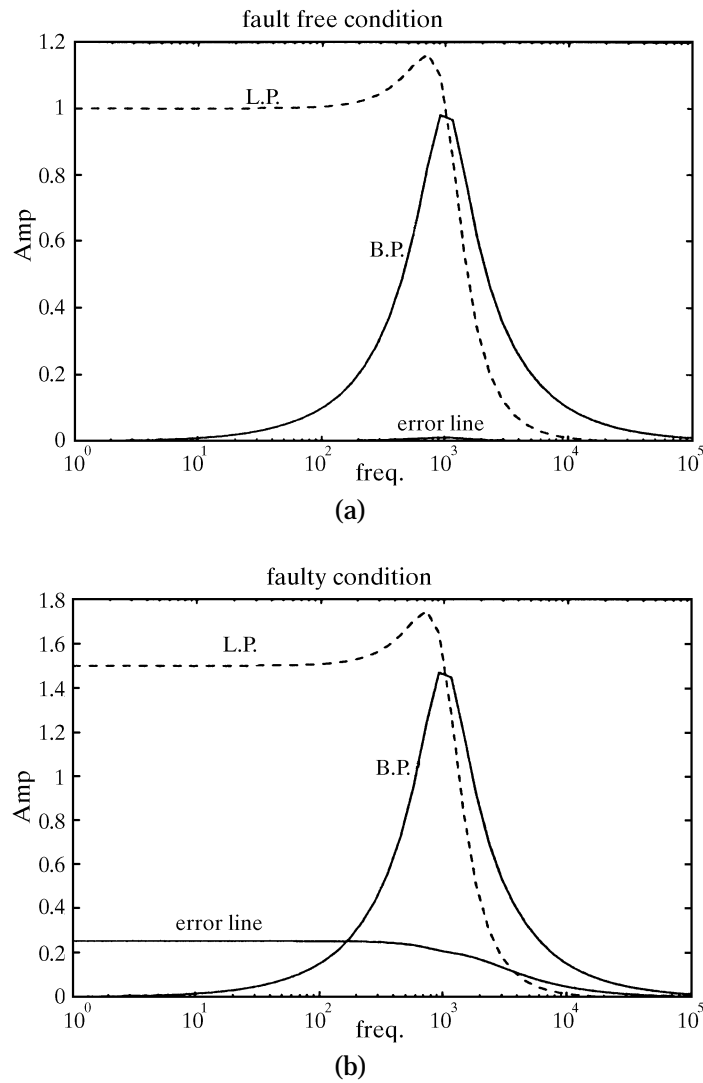


Fig. 5. The responses of CUT and the test circuit (a) under fault free conditions and (b) under faulty conditions.

### 3.2 Relation Between a Fault and the Error Line

In this subsection we discuss how a fault in the CUT affects the error line  $e(z)$ . In the following analysis we use the notation  $SC_i$  to denote the sub-circuit that directly affect state variable  $x_i(z)$ . For example, the sub-circuits  $SC_1$  and  $SC_2$  of Fig. 2 are indicated by dash lines. We next prove the following results.

**Lemma 1:** *In a state variable system, a fault in a component of sub-circuit  $SC_i$  only affects the entries of the  $i$ 'th row of  $\mathbf{A}$  and  $\mathbf{B}$  matrices of the state equation.*

**Proof:** Clearly the sub-circuit  $SC_i$  of a state variable system is the realization of the  $i$ 'th row of the state equation. Hence, a fault in a component of sub-circuit  $SC_i$  will cause only the  $i$ 'th row of the state equation to change.  $\square$

It should be pointed out that Lemma 1 does not imply that a fault in a component of  $SC_i$  will not affect the value of any other state variable, say  $x_j(z)$  ( $j \neq i$ ). In fact the value of  $x_j(z)$  may change, but since the components in  $SC_j$  are fault-free, the  $j$ 'th row of the state equation which relates  $x_j(z)$  to other state variables is not changed.

**Theorem 2:** A fault in a component of the sub-circuit  $SC_i$  can cause the value of the error line to change. The value of the error line depends on the value of  $\alpha_i$  of the coding vector and is independent of  $\alpha_j$  for all  $j \neq i$ .

**Proof:** According to Lemma 1, a fault in a component of sub-circuit  $SC_i$  can only cause the  $i$ 'th row of a state equation to change. We assume that a fault causes the elements  $a_{ij}$  and  $b_{ij}z^{-1}$  in the matrix  $\mathbf{A}''(z)$  to change respectively to  $(a_{ij} + \delta_{ij})$  and  $(b_{ij}z^{-1} + w_{ij}z^{-1})$ ,  $j = 1, 2, \dots, n$ . It also causes the elements  $c_i$  and  $d_i z^{-1}$  in the matrix  $\mathbf{B}''(z)$  to change to  $(c_i + \theta_i)$  and  $(d_i z^{-1} + \phi_i z^{-1})$ , respectively. Hence, the corresponding state equation has the following form:

$$\begin{bmatrix} x_1(z) \\ \vdots \\ x_i(z) \\ \vdots \\ x_n(z) \\ x_{n+1}(z) \end{bmatrix} = \begin{bmatrix} a_{11} + b_{11}z^{-1} & \cdots & a_{1n} + b_{1n}z^{-1} & 0 \\ \vdots & \ddots & \vdots & \vdots \\ (a_{i1} + \delta_{i1}) + (b_{i1} + w_{i1})z^{-1} & \cdots & (a_{in} + \delta_{in}) + (b_{in} + w_{in})z^{-1} & 0 \\ \vdots & \ddots & \vdots & \vdots \\ a_{n1} + b_{n1}z^{-1} & \cdots & a_{nn} + b_{nn}z^{-1} & 0 \\ \gamma_1(z) & \cdots & \gamma_n(z) & 0 \end{bmatrix}$$

$$\begin{bmatrix} \frac{x_1(z)}{1-z^{-1}} \\ \vdots \\ \frac{x_i(z)}{1-z^{-1}} \\ \vdots \\ \frac{x_n(z)}{1-z^{-1}} \\ \frac{x_{n+1}(z)}{1-z^{-1}} \end{bmatrix} + \begin{bmatrix} c_1 + d_1 z^{-1} \\ \vdots \\ (c_i + \theta_i) + (d_i + \phi_i)z^{-1} \\ \vdots \\ c_n + d_n z^{-1} \\ \beta(z) \end{bmatrix} \frac{u(z)}{1-z^{-1}} \quad (4)$$

According to Theorem 1 and the definitions of  $\gamma_1(z)$ ,  $\gamma_2(z)$ , ...,  $\gamma_n(z)$ , and  $\beta(z)$ , we can get the following equation:

$$\begin{aligned}
e(z) &= \gamma_1(z) \frac{x_1(z)}{1-z^{-1}} + \cdots + \gamma_n(z) \frac{x_n(z)}{1-z^{-1}} + \beta(z) \frac{u(z)}{1-z^{-1}} - \alpha_1 x_1(z) - \cdots - \alpha_n x_n(z) \\
&= -\alpha_i [(\delta_{i1} + w_{i1} z^{-1}) \frac{x_1(z)}{1-z^{-1}} + \cdots + (\delta_{in} + w_{in} z^{-1}) \frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1}) \frac{u(z)}{1-z^{-1}}]
\end{aligned}$$

Since state variables  $x_1(z)$ ,  $x_2(z)$ , ...,  $x_n(z)$  are independent of the coding vector, the error line  $e(z)$  depends only on  $\alpha_i$ .  $\square$

Practically speaking, since an analog circuit is considered fault-free as long as its functions are within its normal range, the error line should be excited only when its magnitude is larger than a threshold value. According to Theorem 2, we can adjust the coding vector or the threshold value so that fault effects can be detected by the concurrent error detection circuitry. For example, we can choose a coding vector of [1,1] and assume that the input signal for the circuit in Fig. 2 is a sinusoidal wave with a frequency of 1k Hz. Let the sampling frequency be 128k; then we can get the time-domain response as shown in Fig. 6. Fig. 6(a) is the simulated result under fault-free conditions. The curves labeled x1 and x2 are the output waveforms of the first and second integrators of Fig. 2(a), respectively. The curve labeled e is the response of the test circuit. The error line is almost zero for all time. The response of the filter when capacitor  $A$  changes to 0.15pF is shown in Fig. 6(b). It can be seen that both x1 and x2 become larger than their normal values. The peak value of error line  $e(z)$  is about 0.3V. Thus, we may simply select a voltage close to 0.3V to detect faults that change  $A$  to larger than 0.15pF.

The above example demonstrates how to determine the threshold value given a coding vector and a specific fault. It should be pointed out that, for a given fixed design, the threshold to determine whether faults exist must be applicable to all circuit components. Since different circuit components may have different degrees of affection on the error line, the selection of the coding vector is important. One should make use of Theorem 2 to unify the fault effects of various circuit components, i.e., to make the effects of different circuit components on the error line approximately the same. This, however, may be complex and is beyond the scope of this paper.

#### 4. FAULT DIAGNOSIS

In this section we present the fault diagnosis scheme. For convenience, the state variable  $x_i$  is said to be faulty if faults are contained in sub-circuit  $SC_i$ . Thus we can say that the concurrent error detection scheme can decide whether or not a state variable is correct. This scheme can detect only a state variable in the state variable system because the distance between the fault-free and faulty state vector  $\mathbf{X}''(z)$  of the modified state equation is two (one is  $x_i(z)$  and the other is  $x_{n+1}(z)$ ), where the distance between two circuits is defined as the number of different rows in their state equation representation. If we can increase the distance between the fault-free and faulty state vectors of the modified state variable system then the fault diagnosis and the fault tolerance of the system can be achieved.

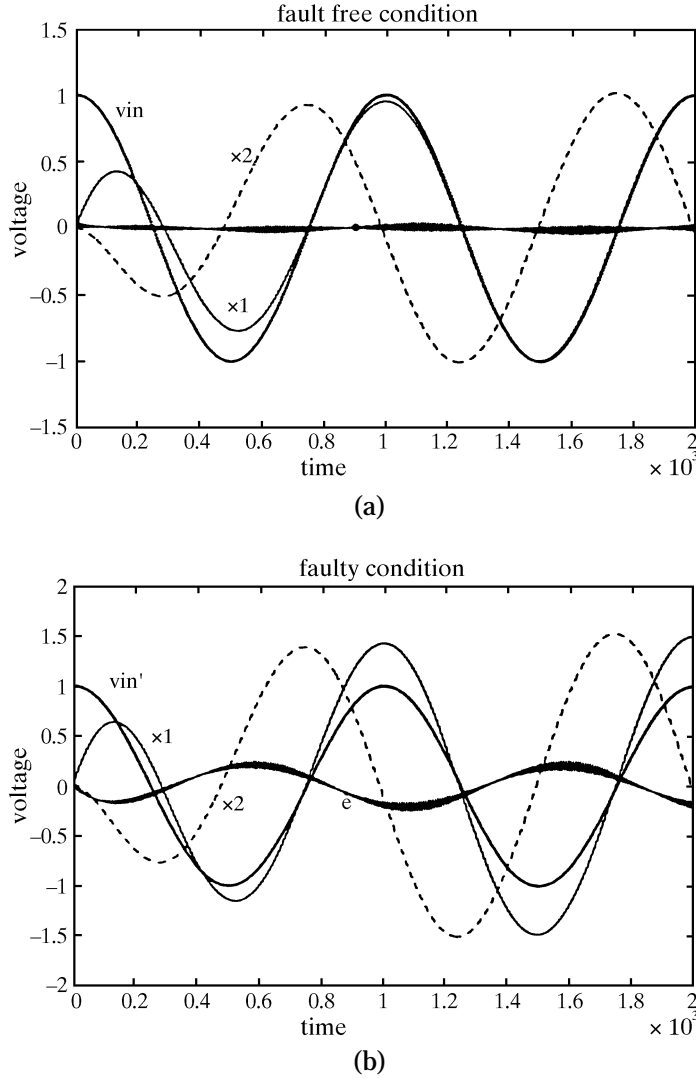


Fig. 6. The time domain responses of CUT and the test circuit under (a) fault free conditions and (b) faulty conditions.

First, we define a new modified state equation  $\tilde{\mathbf{X}}(z) = \tilde{\mathbf{A}}(z) \frac{\tilde{\mathbf{X}}(z)}{1-z^{-1}} + \tilde{\mathbf{B}}(z) \frac{u(z)}{1-z^{-1}}$

where  $\tilde{\mathbf{A}}(z) = \begin{bmatrix} \mathbf{A}'(z) & 0 & 0 \\ \mathbf{A}_1(z) & 0 & 0 \\ \mathbf{A}_2(z) & 0 & 0 \end{bmatrix}$  is an  $(n+2) \times (n+2)$  matrix whose far two right

columns are all zero, and  $\tilde{\mathbf{B}}(z) = \begin{bmatrix} \mathbf{B}'(z) \\ \beta_1(z) \\ \beta_2(z) \end{bmatrix}$  is an  $(n+2) \times 1$  matrix, with  $\mathbf{A}_1(z) = [\gamma_{11}(z),$

$\gamma_{12}(z), \dots, \gamma_{1n}(z) = [\alpha_{11}, \alpha_{12}, \dots, \alpha_{1n}] \cdot \mathbf{A}'(z)$ ,  $\mathbf{A}_2(z) = [\gamma_{21}(z), \gamma_{22}(z), \dots, \gamma_{2n}(z)] = [\alpha_{21}, \alpha_{22}, \dots, \alpha_{2n}] \cdot \mathbf{A}'(z)$ ,  $\beta_1(z) = [\alpha_{11}, \alpha_{12}, \dots, \alpha_{1n}] \cdot \mathbf{B}'(z)$ , and  $\beta_2(z) = [\alpha_{21}, \alpha_{22}, \dots, \alpha_{2n}] \cdot \mathbf{B}'(z)$ . The modified state equation can be expanded as

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ \vdots \\ x_n(z) \\ x_{n+1}(z) \\ x_{n+2}(z) \end{bmatrix} = \begin{bmatrix} a_{11} + b_{11}z^{-1} & \cdots & a_{1n} + b_{1n}z^{-1} & 0 & 0 \\ a_{21} + b_{21}z^{-1} & \cdots & a_{2n} + b_{2n}z^{-1} & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ a_{n1} + b_{n1}z^{-1} & \cdots & a_{nn} + b_{nn}z^{-1} & 0 & 0 \\ \gamma_{11}(z) & \cdots & \gamma_{1n}(z) & 0 & 0 \\ \gamma_{21}(z) & \cdots & \gamma_{2n}(z) & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{x_1(z)}{1-z^{-1}} \\ \frac{x_2(z)}{1-z^{-1}} \\ \vdots \\ \frac{x_n(z)}{1-z^{-1}} \\ \frac{x_{n+1}(z)}{1-z^{-1}} \\ \frac{x_{n+2}(z)}{1-z^{-1}} \end{bmatrix} + \begin{bmatrix} c_1 + d_1z^{-1} \\ c_2 + d_2z^{-1} \\ \vdots \\ c_n + d_nz^{-1} \\ \beta_1(z) \\ \beta_2(z) \end{bmatrix} \frac{u(z)}{1-z^{-1}}$$

To perform fault diagnosis, we must find out the faulty state variable. But first we must distinguish the error due to a fault in the CUT from that in the circuitry for the additional state variables  $x_{n+1}(z)$  and  $x_{n+2}(z)$ . Assume the outputs of the test circuits derived from  $x_{n+1}(z)$  and  $x_{n+2}(z)$  are  $e_1(z)$  and  $e_2(z)$ , respectively. There are four possibilities for  $e_1(z)$  and  $e_2(z)$ : (a)  $e_1(z) = 0$  and  $e_2(z) = 0$ , (b)  $e_1(z) \neq 0$  and  $e_2(z) = 0$ , (c)  $e_1(z) = 0$  and  $e_2(z) \neq 0$ , (d)  $e_1(z) \neq 0$  and  $e_2(z) \neq 0$ . Case (a) is the fault free case. Cases (b) and (c) correspond to faults in test circuits based on  $x_{n+1}(z)$  and  $x_{n+2}(z)$ , respectively. Case (d) occurs when there are faults in the CUT. Clearly cases (b) and (c) are easy to deal with, thus in the following we will concentrate on case (d).

**Theorem 3:** If  $\frac{\alpha_{21}}{\alpha_{11}} \neq \frac{\alpha_{22}}{\alpha_{12}} \neq \dots \neq \frac{\alpha_{2i}}{\alpha_{1i}} \neq \dots \neq \frac{\alpha_{2n}}{\alpha_{1n}}$ , then the faulty state variable  $x_i(z)$  and its associated sub-circuit  $SC_i$  can be properly diagnosed.

**Proof:** According to Theorem 2, if  $x_i(z)$  is faulty (or the fault is contained in  $SC_i$ ), then  $e_1(z) = -\alpha_{1i}f(z)$  where  $f(z) = [(\delta_{i1} + w_{i1}z^{-1})\frac{x_1(z)}{1-z^{-1}} + \dots + (\delta_{in} + w_{in}z^{-1})\frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1})\frac{u(z)}{1-z^{-1}}]$ . Since  $f(z)$  depends only on the faults in CUT, it is the same in  $e_1(z)$  and in  $e_2(z)$ . Thus,  $\frac{e_2(z)}{e_1(z)} = \frac{-\alpha_{2i}f(z)}{-\alpha_{1i}f(z)} = \frac{\alpha_{2i}}{\alpha_{1i}}$ . Therefore,  $\frac{\alpha_{2i}}{\alpha_{1i}}$  can be used as an index to the faulty state variable.  $\square$

To locate the faulty state variable, we use the architecture proposed in [6]. Fig. 7 shows the overall fault diagnosis and error correction architecture. The box T1 (T2) generates a logical '1' on its output line if the peak value of  $e_1(z)$  ( $e_2(z)$ ) is larger than a predetermined threshold. If it is determined that the fault is in the CUT, then the next step is to determine the state variable  $x_i(z)$ , for  $1 \leq i \leq n$ , whose representation in the faulty system is different from that in the fault free system.

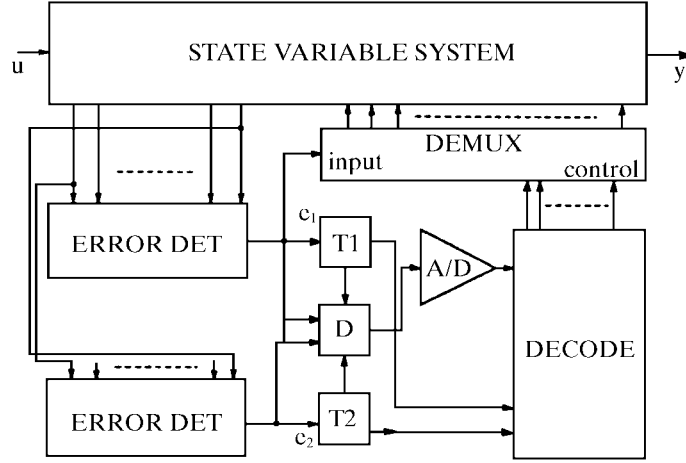


Fig. 7. The error correction architecture.

When a fault exists in the CUT, the analog divider  $D$  of Fig. 7 performs the division  $\frac{e_2(z)}{e_1(z)}$  and outputs one of the values of  $\frac{\alpha_{2i}}{\alpha_{1i}}$ , for some  $1 \leq i \leq n$ . This output is fed to an A/D converter, which generates a digital encoding of the value of  $\frac{\alpha_{2i}}{\alpha_{1i}}$ . The DECODE box connected to the output of the A/D converter then determines the index  $i$  of the faulty state variable  $x_i(z)$  and, thus, fault diagnosis can be achieved. The output of the DECODE box is then used to control an analog demultiplexer (DEMUX) to direct error line  $e_1(z)$  into an appropriate node of the original state variable system (CUT) to achieve error correction. In the case of no fault, the DECODE logic sets the control inputs of the demultiplexer so that all its outputs are connected to ground.

In the next section, we describe in detail how to perform error correction and fault tolerance.

## 5. ERROR CORRECTION AND FAULT TOLERANCE

Consider the modified state equation (Eq. (2)). Assume the error line is excited due to a fault in sub-circuit  $SC_i$  and it is diagnosed correctly by the scheme described in the last section. According to Lemma 1, a fault in sub-circuit  $SC_i$  can only cause the  $i$ 'th row of the state equation to change. Let's again assume a fault in sub-circuit  $SC_i$  causes the  $a_{ij}$  and  $b_{ij}z^{-1}$  in matrix  $\mathbf{A}''(z)$  to change to  $(a_{ij} + \delta_{ij})$  and  $(b_{ij} + w_{ij})z^{-1}$  respectively and causes the  $c_i$  and  $d_i z^{-1}$  in matrix  $\mathbf{B}''(z)$  to change to  $(c_i + \theta_i)$  and  $(d_i + \phi_i)z^{-1}$  respectively, as shown in Eq. (4). Assume coding vector =  $[1, 1, \dots, 1]$ . According to Theorem 2, we have

$$e(z) = - \left[ (\delta_{i1} + w_{i1}z^{-1}) \frac{x_1(z)}{1-z^{-1}} + \dots + (\delta_{in} + w_{in}z^{-1}) \frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1}) \frac{u(z)}{1-z^{-1}} \right]$$

Comparing  $e(z)$  with the  $i$ 'th row of the state equation under a fault in sub-circuit  $SC_i$ , we find that  $e(z)$  is proportional to the deviation of the  $i$ 'th row from its normal condition. If we feed  $-e(z)$  back to  $x_i(z)$  then we can cancel the error due to faults in sub-circuit  $SC_i$ .

Fig. 8 is the signal flow graph of the error correction scheme. By feeding  $e(z)$  into the faulty state variable  $x_i(z)$ , we get

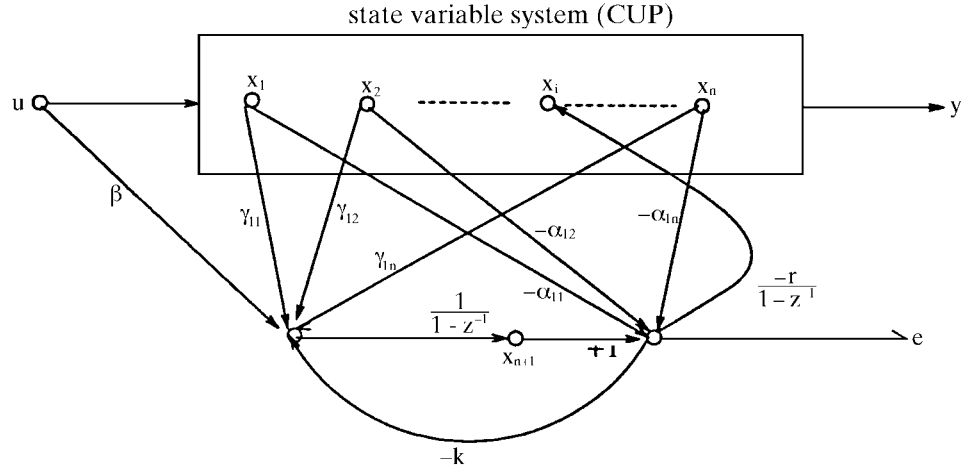


Fig. 8. SFG of error correction.

$$\begin{aligned}
 x_i(z) &= (a_{i1} + \delta_{i1} + b_{i1}z^{-1} + w_{i1}z^{-1}) \frac{x_1(z)}{1-z^{-1}} \\
 &+ \dots \\
 &+ (a_{in} + \delta_{in} + b_{in}z^{-1} + w_{in}z^{-1}) \frac{x_n(z)}{1-z^{-1}} \\
 &+ (c_i + \theta_i + d_i z^{-1} + \phi_i z^{-1}) \frac{u(z)}{1-z^{-1}} - \frac{re(z)}{1-z^{-1}}
 \end{aligned}$$

where  $r$  is the gain of error line. The error line after feeding  $e(z)$  into the faulty state variable  $x_i(z)$  changes to

$$\begin{aligned}
 e(z) &= -[(\delta_{i1} + w_{i1}z^{-1}) \frac{x_1(z)}{1-z^{-1}} + \dots + (\delta_{in} + w_{in}z^{-1}) \frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1}) \frac{u(z)}{1-z^{-1}}] \\
 &+ \frac{re(z)}{1-z^{-1}} - \frac{ke(z)}{1-z^{-1}}
 \end{aligned}$$

Rearranging the last equation, we get

$$(1 - \frac{r}{1-z^{-1}} + \frac{k}{1-z^{-1}})e(z) = -[(\delta_{i1} + w_{i1}z^{-1})\frac{x_1(z)}{1-z^{-1}} + \dots + (\delta_{in} + w_{in}z^{-1})\frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1})\frac{u(z)}{1-z^{-1}}]$$

If  $k \ll 1$  and  $r \gg 1$  then

$$-\frac{re(z)}{1-z^{-1}} = -[(\delta_{i1} + w_{i1}z^{-1})\frac{x_1(z)}{1-z^{-1}} + \dots + (\delta_{in} + w_{in}z^{-1})\frac{x_n(z)}{1-z^{-1}} + (\theta_i + \phi_i z^{-1})\frac{u(z)}{1-z^{-1}}]$$

Thus if we make  $r$  large,  $e(z)$  can be reduced to a small value.

Fig. 9 is the signal flow graph of Fig. 2 with error correction. In Fig. 10 the connection between  $e(z)$  and the faulty state variable  $x_1(z)$  for Fig. 2 is added to the original circuit. The SWITCAP simulation results after correction are shown in Fig. 11. It can be seen that the error has been reduced and the error correction is achieved. Because the system can still work correctly even if faults exist in it, fault tolerance is achieved. Fig. 12 is the time domain response after feeding  $e(z)$  into  $x_1(z)$ .

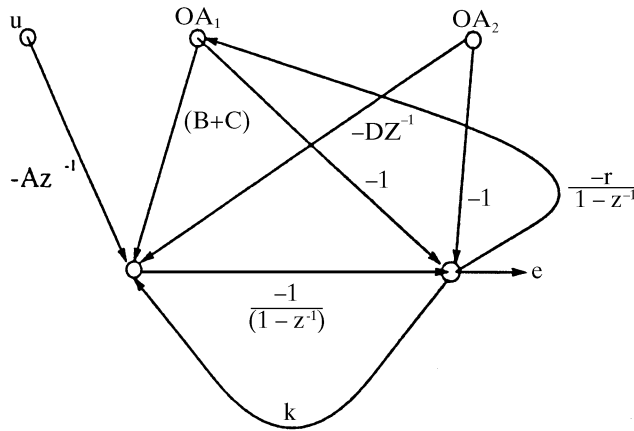


Fig. 9. SFG of the biquadratic filter with error correction.

One important thing that must be kept in mind is that the above results are valid only when two consecutive output values are close to each other, i.e., when the ratio  $\frac{f_c}{f}$  is large, where  $f_c$  is the sampling frequency for the switches and  $f$  is the frequency of the input signal. In fact, from the time domain point of view the error correction scheme always corrects the values in the previous clock cycle and hence if the ratio of  $\frac{f_c}{f}$  is small, the effectiveness of this scheme will be reduced.

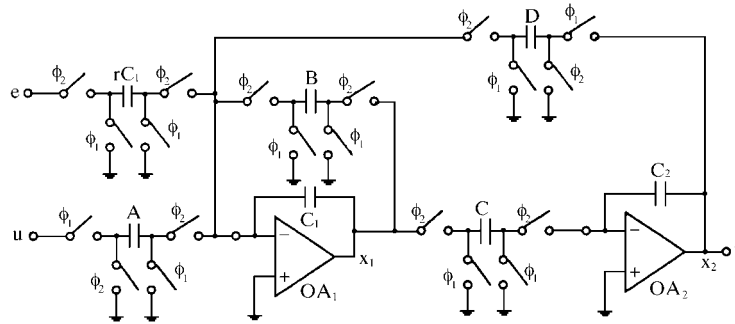


Fig. 10. Circuit connection for error correction.

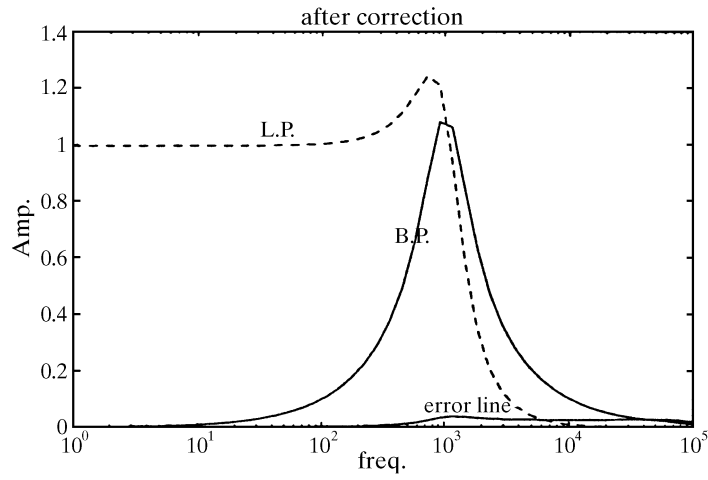


Fig. 11. The response of CUT and the test circuit after correction.

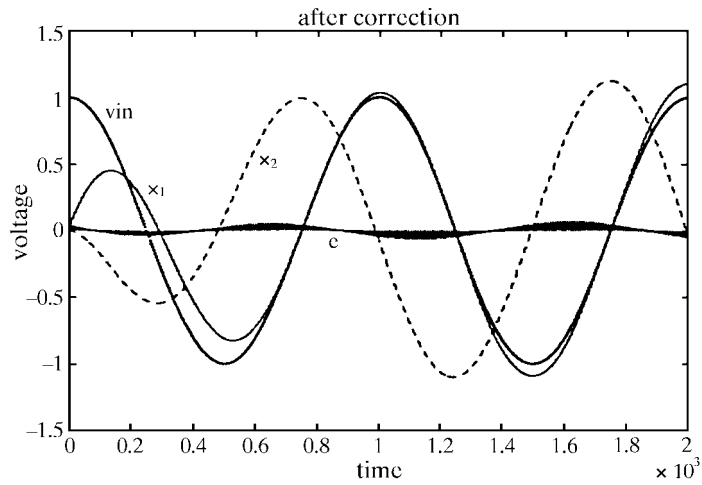


Fig. 12. The time domain response of CUT and the test circuit after correction.

### 6. SIMPLIFICATION RULES OF TEST CIRCUITS

The test circuitry is small in comparison with the CUT because it only needs one op-amp for each additional row. Compared with the scheme which duplicates CUT to perform concurrent testing our method requires much less area overhead. However, further reduction of overhead is possible as described below.

The simplification rules we used are shown in Fig. 13 [10]. Since the transfer functions of the inverting and non-inverting integrators are  $-\frac{c_1}{1-z^{-1}}$  and  $\frac{c_2 z^{-1}}{1-z^{-1}}$  respectively, if the two integrators have the same input source  $V_S$  and their other terminals are connected to the virtual ground  $V_G$  of the same op amp (op amp is omitted here), then the transfer function of this circuit is

$$H(z) = -\frac{c_1}{1-z^{-1}} + \frac{c_2 z^{-1}}{1-z^{-1}} \tag{5}$$

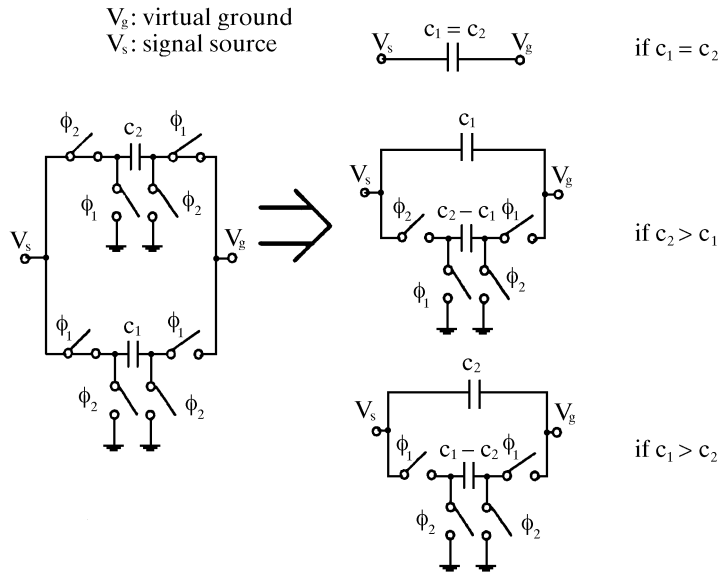


Fig. 13. The simplification rules of switched-capacitor circuits.

Depending on the capacitance value of  $c_1$  and  $c_2$ , Eq. (5) can be simplified as shown in the following three cases.

**Case (1):**  $c_1 = c_2$  For this condition, Eq. (5) becomes  $H(z) = -c_1$ . It can be implemented by a capacitor with a value  $c_1$ . In this case, one capacitor and all the switches can be eliminated.

**Case (2):**  $c_2 > c_1$  For this condition, Eq. (5) becomes  $H(z) = -c_1 + \frac{(c_2 - c_1)z^{-1}}{1 - z^{-1}}$ . It can be implemented by a capacitor with the capacitance value  $c_1$  and a

non-inverting integrator with the capacitance value  $(c_2 - c_1)$ . The original total capacitance value is  $(c_1 + c_2)$ , but after simplification the total capacitance value will become  $c_1 + (c_2 - c_1) = c_2$ . In addition, four switches are saved.

**Case (3):**  $c_1 > c_2$  This condition is similar to **Case (2)**. Eq. (5) will become  $H(z) = -c_2 - \frac{(c_1 - c_2)}{1 - z^{-1}}$  and can be implemented by a capacitor with the capacitance value  $c_2$  and an inverting integrator with the capacitance value  $(c_1 - c_2)$ . The total capacitance value saved is  $c_2$  and four switches are eliminated.

## 7. CASE STUDY

In this section we use a practical SC filter to illustrate the methodology described in the previous sections. Fig. 14 is a fifth-order, low-pass Chebyshev filter [12]. The signal flow graph of this filter is shown in Fig. 15. The capacitor  $c_i$ ,  $1 \leq i \leq 5$ , is 3pF and capacitors  $\alpha_{31}c$  and  $\alpha_{ij}c$ ,  $i = 1$  or  $2$  and  $1 \leq j \leq 5$ , are 0.1pF. The sampling frequency is 128kHz. Assume coding vectors are  $[1, 1, 1, 1, 1]$  and  $[1, 2/3, 1/2, 2/5, 1/3]$ , then the modified state equation

$\tilde{\mathbf{X}}(z) = \tilde{\mathbf{A}}(z) \frac{\tilde{\mathbf{X}}(z)}{1 - z^{-1}} + \tilde{\mathbf{B}}(z) \frac{u(z)}{1 - z^{-1}}$  is

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ x_3(z) \\ x_4(z) \\ x_5(z) \\ x_6(z) \\ x_7(z) \end{bmatrix} = \begin{bmatrix} -\frac{\alpha_{31}}{c_1} & -\frac{\alpha_{21}}{c_1} & 0 & 0 & 0 & 0 & 0 \\ \frac{\alpha_{12}z^{-1}}{c_2} & 0 & -\frac{\alpha_{22}}{c_{22}} & 0 & 0 & 0 & 0 \\ 0 & \frac{\alpha_{13}z^{-1}}{c_3} & 0 & -\frac{\alpha_{23}}{c_3} & 0 & 0 & 0 \\ 0 & 0 & \frac{\alpha_{14}z^{-1}}{c_4} & 0 & -\frac{\alpha_{24}}{c_4} & 0 & 0 \\ 0 & 0 & 0 & \frac{\alpha_{15}z^{-1}}{c_5} & -\frac{\alpha_{25}}{c_5} & 0 & 0 \\ (\frac{\alpha_{12}z^{-1}}{c_2} - \frac{\alpha_{31}}{c_1}) & (\frac{\alpha_{13}z^{-1}}{c_3} - \frac{\alpha_{21}}{c_1}) & (\frac{\alpha_{14}z^{-1}}{c_4} - \frac{\alpha_{22}}{c_2}) & (\frac{\alpha_{15}z^{-1}}{c_5} - \frac{\alpha_{23}}{c_3}) & (-\frac{\alpha_{25}}{c_5} - \frac{\alpha_{24}}{c_4}) & 0 & 0 \\ (\frac{2}{3}\frac{\alpha_{12}z^{-1}}{c_2} - \frac{\alpha_{31}}{c_1}) & (\frac{1}{2}\frac{\alpha_{13}z^{-1}}{c_3} - \frac{\alpha_{21}}{c_1}) & (\frac{2}{5}\frac{\alpha_{14}z^{-1}}{c_4} - \frac{2}{3}\frac{\alpha_{22}}{c_2}) & (\frac{1}{3}\frac{\alpha_{15}z^{-1}}{c_5} - \frac{1}{2}\frac{\alpha_{23}}{c_3}) & (-\frac{1}{3}\frac{\alpha_{25}}{c_5} - \frac{2}{5}\frac{\alpha_{24}}{c_4}) & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} x_1(z) \\ x_2(z) \\ x_3(z) \\ x_4(z) \\ x_5(z) \\ x_6(z) \\ x_7(z) \end{bmatrix} \frac{1}{1 - z^{-1}} + \begin{bmatrix} \frac{\alpha_{11}z^{-1}}{c_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{\alpha_{11}z^{-1}}{c_1} \\ \frac{\alpha_{11}z^{-1}}{c_1} \end{bmatrix} \frac{u(z)}{1 - z^{-1}}$$

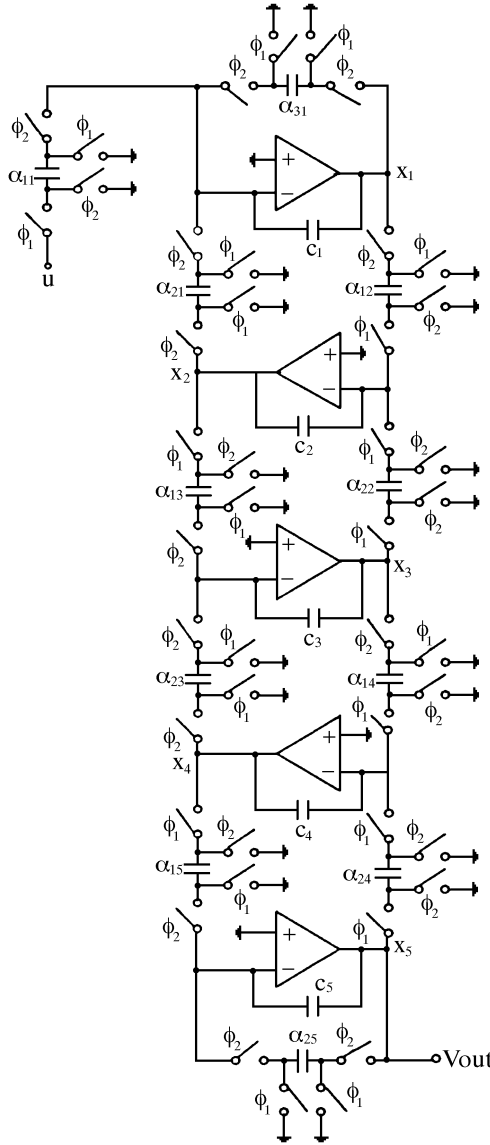


Fig. 14. The fifth order low-pass Chebyshev filter.

In the above equation, the first 5 rows represent the state equation of the 5th order filter and the lowest two rows are used to construct the test circuitry. According to  $e_1(z) = (\frac{\alpha_{12}z^{-1} - \alpha_{31}}{c_2} \frac{x_1(z)}{1 - z^{-1}} + (\frac{\alpha_{13}z^{-1} - \alpha_{21}}{c_3} \frac{x_2(z)}{1 - z^{-1}} + (\frac{\alpha_{14}z^{-1} - \alpha_{22}}{c_4} \frac{x_3(z)}{1 - z^{-1}} + (\frac{\alpha_{15}z^{-1} - \alpha_{23}}{c_5} \frac{x_4(z)}{1 - z^{-1}} + (-\frac{\alpha_{25}z^{-1} - \alpha_{24}}{c_4} \frac{x_5(z)}{1 - z^{-1}} + \frac{\alpha_{11}z^{-1} u(z)}{1 - z^{-1}} - [x_1(z) + x_2(z) + x_3(z) + x_4(z) + x_5(z)]$  and  $e_2(z) = (\frac{2}{3} \frac{\alpha_{12}z^{-1} - \alpha_{31}}{c_2} \frac{x_1(z)}{1 - z^{-1}} + (\frac{1}{2} \frac{\alpha_{13}z^{-1} - \alpha_{21}}{c_3} \frac{x_2(z)}{1 - z^{-1}} +$

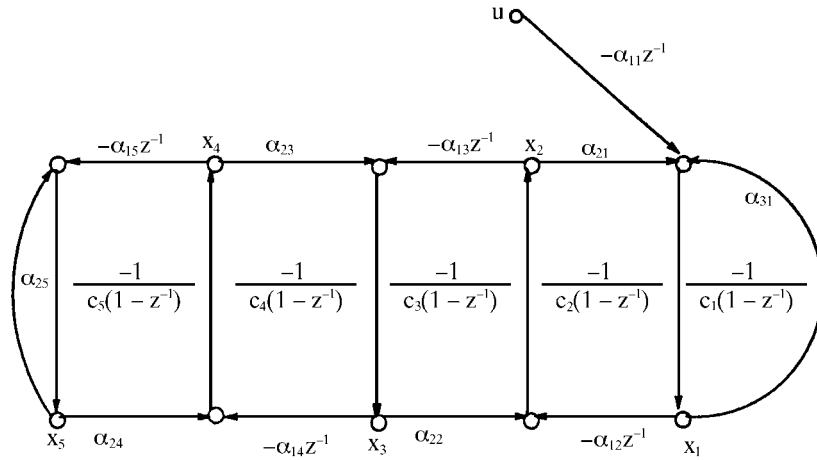


Fig. 15. SFG of the fifth order low-pass Chebyshev filter.

$$\left(\frac{2}{5} \frac{\alpha_{14}}{c_4} z^{-1} - \frac{2}{3} \frac{\alpha_{22}}{c_2}\right) \frac{x_3(z)}{1-z^{-1}} + \left(\frac{1}{3} \frac{\alpha_{15}}{c_5} z^{-1} - \frac{1}{2} \frac{\alpha_{23}}{c_3}\right) \frac{x_4(z)}{1-z^{-1}} + \left(\frac{1}{3} \frac{\alpha_{25}}{c_5} - \frac{2}{5} \frac{\alpha_{24}}{c_4}\right) \frac{x_5(z)}{1-z^{-1}} + \frac{\alpha_{11}}{c_1} z^{-1} \frac{u(z)}{1-z^{-1}} - [x_1(z) + \frac{2}{3}x_2(z) + \frac{1}{2}x_3(z) + \frac{2}{5}x_4(z) + \frac{1}{3}x_5(z)]$$
 we can design the test circuitry for the fifth order Chebyshev filter. The signal flow graph to generate  $e_1(z)$  is shown in Fig. 16, where  $\beta = -\alpha_{11}z^{-1}$ ,  $\gamma_1 = \alpha_{31} - \alpha_{12}z^{-1}$ ,  $\gamma_2 = \alpha_{21} - \alpha_{13}z^{-1}$ ,  $\gamma_3 = \alpha_{22} - \alpha_{14}z^{-1}$ ,  $\gamma_4 = \alpha_{23} - \alpha_{15}z^{-1}$ , and  $\gamma_5 = \alpha_{24} + \alpha_{25}$ . The test circuitry is shown in Fig. 17, where  $cc = cc_i = 3\text{pF}$  for  $1 \leq i \leq 5$  and  $k = 0.1$ . The simulation result under fault free conditions is shown in Fig. 18(a). If a fault causes the capacitor  $\alpha_{11}$  to change to  $0.15\text{pF}$ , then the simulation result is shown in Fig. 18(b). Fig. 18(c) is the result when we feed  $e_1(z)$  into the faulty state variable. It shows that the effects of the fault in the CUT have been reduced.

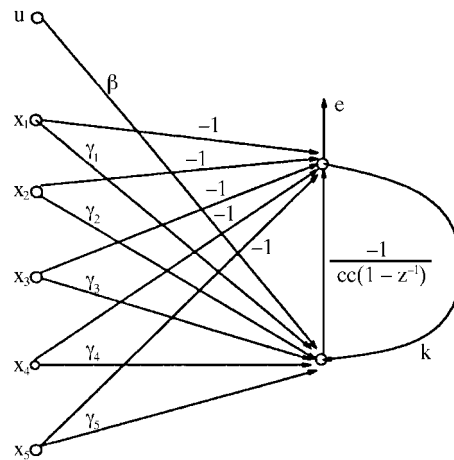


Fig. 16. SFG of the test circuitry.

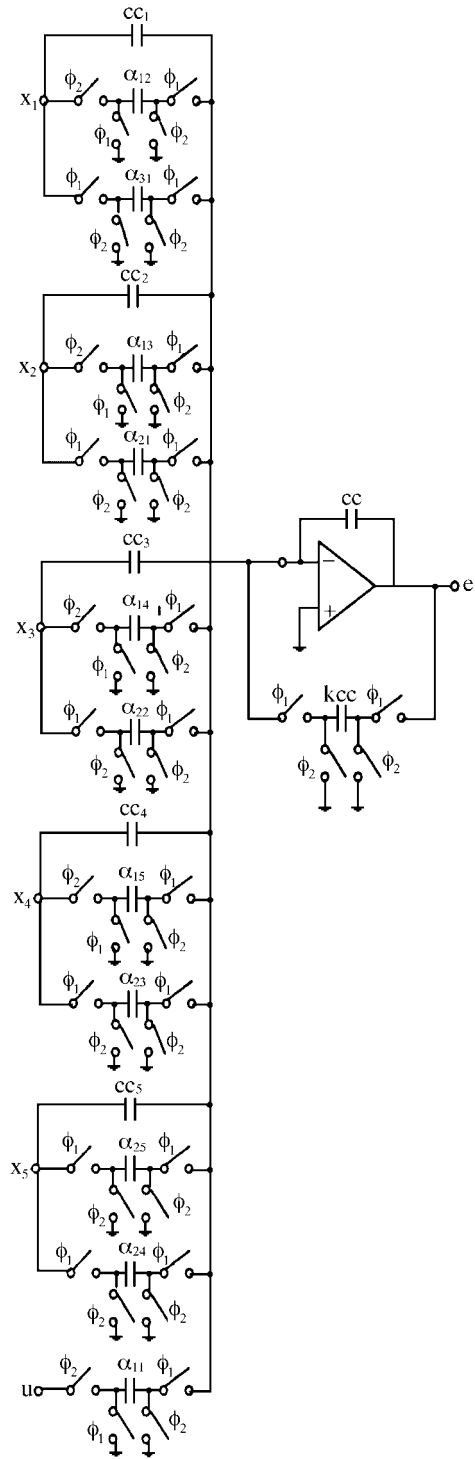


Fig. 17. Test circuitry for the fifth order Chebyshev filter.

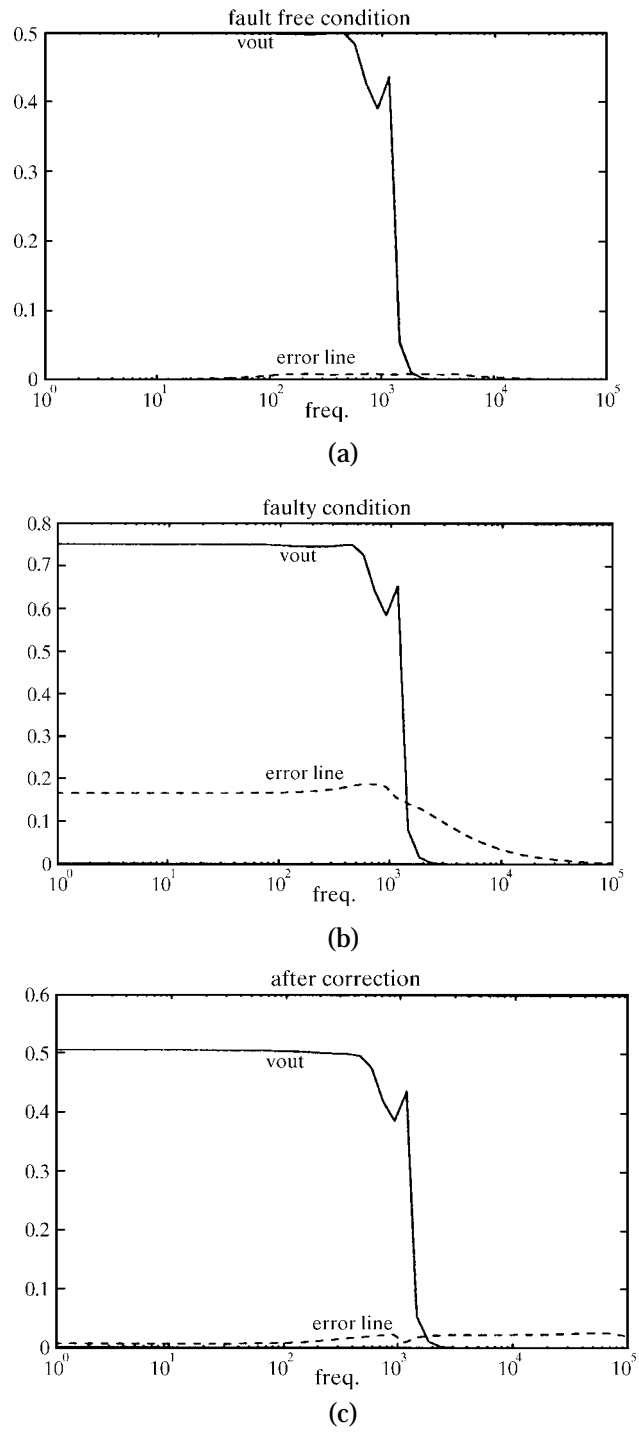


Fig. 18. The responses of the fifth order Chebyshev filter and error line (a) under fault free conditions, (b) under faulty conditions, and (c) after error correction.

By observing Fig. 17, we find that many parts of the test circuit have similar structures and, hence, can be merged and simplified. By applying the simplification rules given in Fig.13 to Fig. 17 of the previous section, we can get the simplified test circuitry shown in Fig. 19, which is clearly much simpler than Fig. 17.

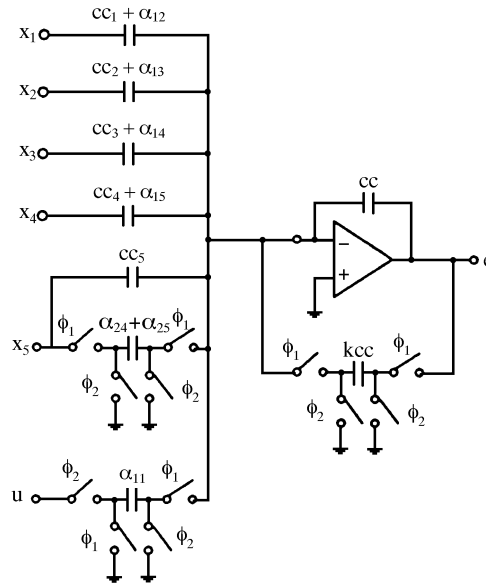
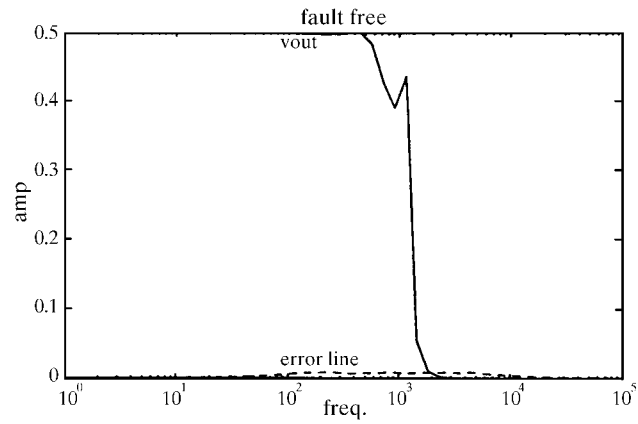
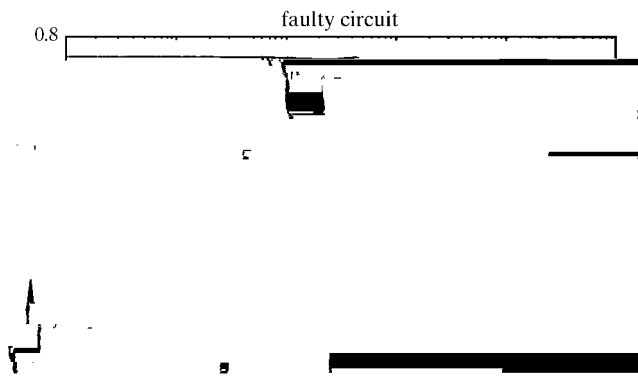


Fig. 19. The simplified test circuitry.

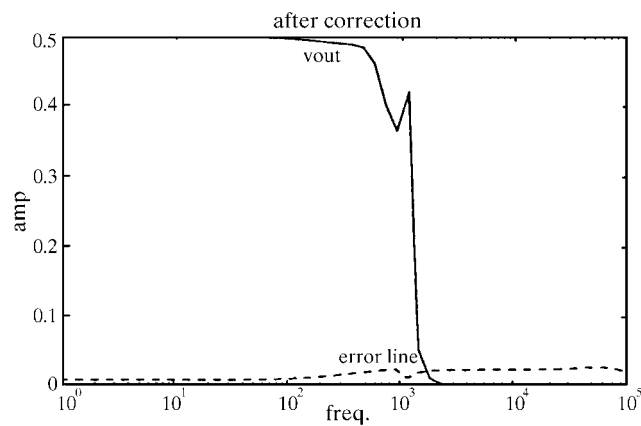
The following simulation uses the simplified test circuitry shown in Fig. 19. The simulation result under fault free conditions is shown in Fig. 20(a). The simulation result for a fault causing the capacitor  $\alpha_{11}$  to change to 0.15pF is shown in Fig. 20(b). Fig. 20(c) is the result when we feed  $e_1(z)$  into the faulty state variable. All these simulation results are almost the same as those before the simplification rules are applied.



(a)



(b)



(c)

Fig. 20. The responses of the filter and error line with the simplified test circuit (a) under fault free conditions, (b) faulty conditions, and (c) after correction.

There does exist one problem that requires further study: in this paper we did not elaborate on the selection of the coding vectors. For example, we only use [1, 1, ..., 1] for error detection. Clearly, different circuit components in a SCF may have different fault effects on the error indication as well as on the output of the SCF. From a practical point of view, high correlation between the circuit output deviation and the error line voltage is desired. Hence, how to identify a coding vector so that these two factors can be closely related, preferably in a linear relationship, deserves further study.

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