

Short Paper

A Probabilistic Model for Path Delay Fault Testing

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Testing path delay faults (PDFs) in VLSI circuits is becoming an important issue as we enter the deep submicron age. However, it is difficult in general since the number of faults is normally very large and most faults are either hard to sensitize or are untestable. In this paper, we propose a probabilistic PDF model. We investigate probability functions for the wire and path delay size to model the fault effect in the circuit under test. In our approach, the delay fault size is assumed to be randomly distributed. An analytical model is proposed to evaluate the PDF coverage. We show that the delay sizes of the untested paths are actually reduced if these paths are conjoined with other tested good paths. Therefore, using our approach, path selection and synthesis of PDF testable circuits can be done more accurately. Also, given a test set, more accurate fault coverage can be predicted by calculating the mean delay of the paths.

Keywords: digital testing, path delay fault, robust test, synthesis for testability, transition fault

1. INTRODUCTION

With the advent of deep-submicron VLSI technology, the clock speed of general logic chips will soon reach the giga-hertz level. While the clock period is being shortened, the issue of accuracy is becoming increasingly important. Faults caused by an excessive propagation delay beyond the specified tolerance are called *delay faults*. Two major delay fault models have been proposed and extensively studied [1-12]. The *gate delay fault* (GDF) model assumes that the delay defects are lumped at a faulty gate and can be tested by propagating the defect to an observable output via any path [1]. This is similar to the classical stuck-at fault model [13] and assumes that the timing delay is solely due to the fault effect of some gate. Test patterns for stuck-at faults, thus, can be adapted to GDFs. Unfortunately, GDFs cannot model distributed delay failures. In contrast to GDFs, the *path delay fault* (PDF) model assumes that the excessive delay is distributed along the faulty path [2]. It seems that all the paths should be verified to guarantee that a complete test can be performed. However, since in the worst case, the total number of paths grows exponentially with the circuit depth, the complexity of such an exhaustive test is prohibitively high. In practice, only a small portion of the paths can be tested explicitly. This raises two questions: First, how can we determine the set of paths to be tested explicitly? Second, how can we determine the fault coverage? A set of paths covering all the wires in the circuit

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under test (CUT) is considered in [14]. The set contains at least a maximum-delay path through every wire in the CUT. In [4], the authors simply select a certain number of the longest (critical) paths. However, in both cases the number may still be large, and high fault coverage cannot be guaranteed. A nonenumerative test generation method [15] has been used to reduce the size of the test set. Since the test generation is based on the circuit structure, a generated test sequence is more effective than a randomly generated one such as that proposed in [16]. Both methods still do not guarantee high fault coverage when the test set is small. As for the method we can use to evaluate the fault coverage of a test set, path delay fault simulation is known to be difficult [17] since a fault is distributed along an entire path. Moreover, there are random defects in the VLSI process, so just as with analog faults, the PDF normally has a randomly distributed fault size.

In this paper, a probabilistic model for path delay fault testing is proposed. We investigate the probability functions of the delay size and simulate the fault effect on paths and segments in the CUT. Instead of using traditional fault simulation techniques [1], we propose a new approach to evaluating the fault coverage by means of probability analysis. In our approach, the delay size is not a constant value but is randomly distributed, and the fault count is replaced by the fault probability of the paths, where the fault probability of a path is the probability that the path delay is longer than the clock period. Given a test set, we can calculate the expected value of the tested faults, and the fault coverage can then be evaluated based on the ratio of the number of tested faults to the total number of faults. The expected delay size of each path can be derived by using an analytical model, leading to more accurate fault coverage analysis. Intuitively, a longer path has a longer expected delay, so we choose paths which are as long as possible in order to have higher fault coverage. Note that we assume that identification of false paths and untestable faults has been done (see, e.g., [12]). We show that there is correlation among different paths if they are *conjoined*; i.e., they share common wires or segments. In this a case, the mean delay size of an untested path will be lower than its original expected value if the path is conjoined with other tested paths that are known to be good. Conditional probability can be used to derive the new probability distribution of the paths for more accurate path selection.

2. PATH DELAY FAULT TESTING

A test for a PDF is a two-pattern sequence $\langle V_1, V_2 \rangle$, where V_1 is the initialization pattern and V_2 is the transition activation pattern. We use the *equivalent normal form* (ENF) expression for the CUT [10]. The ENF of a primary output y of a sensitized path π starting from a primary input x can be written as follows:

$$y_\pi = x \cdot F_1 + \bar{x} \cdot F_2 + G, \quad (1)$$

where F_1 , F_2 , and G are all boolean formulas independent of x . A necessary condition for hazard-free robust testing of π is $G = S0$ (i.e., static zero). However, finding such a test is difficult in general. Also, there is a high percentage of untestable faults in most circuits [6, 12]. To improve the fault coverage, nonrobust tests (NRTs) may be used though they do not guarantee exact fault coverage. Validatable NRTs (VNRTs) [18] can be used to improve the test quality and reliability. An approach to identifying redundant paths and high quality NRTs can be found in [19, 20]. Techniques for designing robustly testable circuits have

also been proposed [7, 10, 21]. Even if a circuit is robustly testable or a BIST structure is used [22], the number of paths is normally large, and sometimes extremely large. The figures for ISCAS-85 benchmark circuits are listed in Table 1. The number of paths directly determines the time required to completely test the CUT. Fortunately, we do not need to do a complete test in almost all cases [4, 12, 14, 23]. However, finding a small subset of paths to be tested which can achieve high fault coverage is not trivial.

Table 1. Numbers of gates and paths for ISCAS-85 benchmarks.

Circuit	Number of gates	Number of paths
c17	6	11
c432	160	83936
c499	202	9440
c880	383	8642
c1355	546	4173216
c1908	880	729057
c2670	1193	679960
c3540	1664	28676671
c5315	2307	1341305
c6288	2416	9.9×10^{19}
c7552	3512	726494

How do we evaluate or predict the fault coverage for the subset of paths to be tested? Conventional simulators count the number of tested good paths only. However, a longer path is more likely to fail than a shorter one. Instead of a fixed value, the delay size of a path should be described by a probability distribution function for a more accurate analysis [9, 20, 24].

3. DELAY SIZE DISTRIBUTION

A path is composed of a chain of *segments*. Each segment may contain a number of cascaded gates and wires. Without loss of generality, we consider only positive delays. Also, although the delay size has a continuous distribution, we approximate it with a discrete distribution to simplify our discussion. We define x as a positive random variable representing the delay size and $f(x)$ as the probability function (or probability distribution) of x for a segment. The function $f(x)$ is closely related to the process quality of the VLSI foundry and can be determined empirically. We further assume that segments of the same length have the same probability function $f(x)$, and that the delay sizes of different segments are mutually independent.

Let $f_1(x_1)$ and $f_2(x_2)$ denote the probability functions of the delay size for two different segments, with mean delays μ_1 and μ_2 and variances σ_1^2 and σ_2^2 , respectively. If we cascade these two segments to form a longer one with a composite probability function $f(x)$ for $x = x_1 + x_2$, then $f(x)$ is the convolution of $f_1(x_1)$ and $f_2(x_2)$, i.e.,

$$f(x) = \sum_{t=0}^x f_1(t)f_2(x-t). \tag{2}$$

Also, $\mu = \mu_1 + \mu_2$ and $\sigma^2 = \sigma_1^2 + \sigma_2^2$ (since x_1 and x_2 are independent). In general, for a path composed of n cascaded segments with mutual independent delay sizes x_1, x_2, \dots, x_n , means $\mu_1, \mu_2, \dots, \mu_n$, variances $\sigma_1^2, \sigma_2^2, \dots, \sigma_n^2$, and probability functions f_1, f_2, \dots, f_n , the mean and variance of the path are $\mu = \sum_{i=1}^n \mu_i$ and $\sigma^2 = \sum_{i=1}^n \sigma_i^2$, respectively. The probability function of the whole path can be derived as follows:

1. $h_2(x) = \sum_{t=0}^x f_1(t)f_2(x-t)$;
2. for ($i = 3$ to n) $h_i(x) = \sum_{t=0}^x h_{i-1}(t)f_i(x-t)$;
3. $f(x) = h_n(x)$.

Note that this procedure can be reversed to calculate the primitive $f_i(x)$ from $f(x)$.

Now let $f_\pi(x)$ be the probability function of the delay for a path π , then, the probability that the delay of π is at least s is

$$P(x \geq s) = \sum_{x \geq s} f_\pi(x), \tag{3}$$

and the probability that the path π is fault free (called the *good probability* of π) is

$$p_\pi \equiv P(x \leq T) = \sum_{x \leq T} f_\pi(x), \tag{4}$$

where T is the clock period. Note that all the segments are assumed to have the same probability function with mean μ and variance σ^2 . The simulation results for p_π over a range of path lengths are shown in Fig. 1, where ‘clk’ stands for the clock period in terms of the number of unit delays and the mean delay of a segment is assumed to be $\mu = 15$ unit delays. The path length is given in terms of the number of levels (segments with single gate). The actual unit delay depends on the CUT, segment, technology, etc., and is of no interest to us in this discussion. From the figure, we can see that paths of mean delay smaller than the clock period have a value of p_π close to 1, and that paths of mean delay larger than the clock period have a p_π value close to 0.

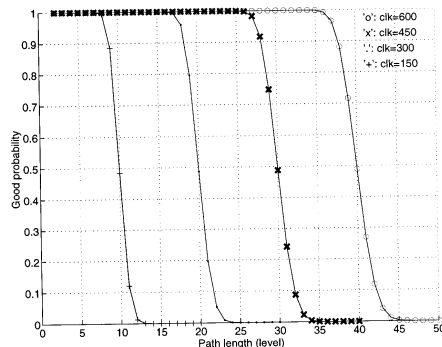


Fig. 1. Good probability for different path lengths and clock periods.

We are also interested in knowing how the variance of the delay size affects p_π . Fig. 2 shows the curves of good probability (p_π) vs. path length (in terms of levels) for different variance values. In the figure, the variance is assumed to be 4, 9, 16, 25, and 36 unit delays, respectively. It can be seen that, though the variance has an impact on p_π , the effect is small.

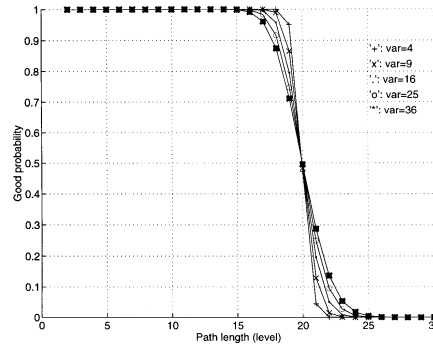


Fig. 2. Good probability for different path lengths and variances.

Table 2 lists the simulation results for ISCAS-85 benchmarks, in which L represents the maximum level (depth) among the critical paths, n_π the number of paths, α_π the ratio of the longest paths selected among the set of all paths, n_f the equivalent number of faults to be tested, and ϕ the fault coverage for the longest paths selected, respectively. Note that the *equivalent fault count* (n_f) is defined as the normalized number of faults calculated by accumulating the $1 - p_\pi$ values of all the paths. Since the $1 - p_\pi$ values are smaller for shorter paths, they contribute less to n_f than do those for the longer paths. The equivalent fault count can be considered as the expected fault count (the size of the fault list) of a CUT when delay-fault testing is performed. We use n_f instead of taking the product $n_\pi \times \alpha_\pi$ directly when we evaluate the fault coverage. In our fault coverage (ϕ) simulation using the

Table 2. The simulation results of benchmark circuits.

Circuit	L	n_π	α_π	n_f	ϕ
c17	3	11	0.55	2.82	0.99
c432	17	83926	0.052	3964.6	0.41
c499	11	9440	0.33	1301.1	0.94
c880	24	8642	0.012	103.4	0.37
c1355	24	4173216	0.047	174948.0	0.39
c1908	40	729057	0.000044	215.4	0.047
c2670	32	679960	0.00075	1441.7	0.12
c3540	47	28676671	0.000003	1034.4	0.028
c5315	49	1341305	0.000009	138.3	0.025
c6288	124	9.9×10^{19}	6.5×10^{-10}	3.16×10^{13}	0.00041
c7552	43	726494	0.00001	86.4	0.025

probabilistic model, we assume that $\sigma = 4$ and $\mu = 15$ for a single segment, and that the clock period is slightly (2%) longer than the mean delay of the critical path. In general, a longer path has a lower p_π value. From Table 2, we can see that testing the few longest paths is not always very effective. However, more paths result in a higher testing cost, and there is a high percentage of untestable paths that need not be tested in many cases [12]. In addition to false paths and untestable paths, we need a simple way to determine the number of paths that should be tested to achieve effective fault coverage and to obtain guidance in path selection.

4. CONJOINED PATHS

In this section, we will go one step further and consider conjoined paths, i.e., paths sharing common segments. Let $f(x)$ be the probability function of the delay size for a segment, and let A denote the independent event for which a path π containing the segment is confirmed fault free. Under the event A , where its probability $P(A) > 0$, we expect that the real probability of delay size x will be different from the original one. The original probability function $f(x)$ is now replaced by the conditional probability function

$$f(x|A) = \frac{f(x)P(A|x)}{P(A)}, \quad (5)$$

where $P(A|x)$ denotes the good probability of path π when the segment delay is x . Let μ and μ_c denote the mean values of $f(x)$ and $f(x|A)$, respectively. We can make the following observations.

First, since the delay size x is independent of the event A , we have

$$\begin{cases} x > \mu \Rightarrow P(A|x) < P(A), & f(x|A) < f(x); \\ x = \mu \Rightarrow P(A|x) = P(A), & f(x|A) = f(x); \\ x < \mu \Rightarrow P(A|x) > P(A), & f(x|A) > f(x). \end{cases} \quad (6)$$

From (6), e.g., if $x > \mu$, the segment is worse than average, so $P(A|x) < P(A)$ and $f(x|A) < f(x)$ according to (5).

Second, $\mu_c < \mu$ as shown in Fig. 3, where the curve for $f(x|A)$ (solid line) is to the left of that of $f(x)$ (dotted line). Note that continuous probability density functions have been used in the figure instead of their discrete approximations. Also, we assume normal distribution for the delay size here. It can be shown that the function $f(x|A)$ has smaller mean and variance than the original function $f(x)$. For example, if the original mean and variance for the delay of a segment are 15 and 16, respectively (dotted), then the modified mean and variance for a segment in a tested good path of depth 10 are about 14 and 14.5, respectively (solid). Note that the curves for $f(x|A)$ and $f(x)$ intersect at $x = \mu$ (15 in this example).

The above result is important in that if path π is tested and confirmed good, then for any segment in π , we should consider the conditional probability function $f(x|A)$ instead of $f(x)$. Segments in a tested good path are more likely to have smaller mean and variance. Therefore, if an untested path is conjoined (i.e., shares some segments) with tested good paths, its mean and variance are reduced and its good probability increased. In other words, a tested good path may reduce the fault probability of other paths.

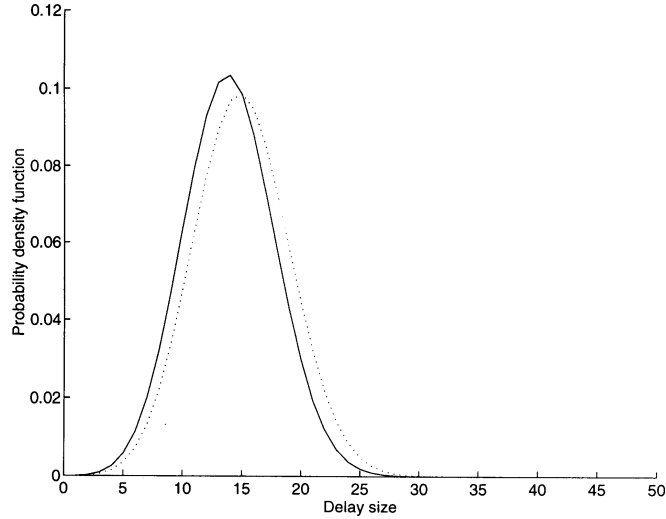


Fig. 3. Curves for $f(x|A)$ (solid) and $f(x)$ (dotted).

Let M_c denote the calculated new mean of the delay size for an untested path conjoined with some tested good path, and let M denote its original mean. Then the normalized path length is defined as

$$L_n = \frac{M_c}{M}. \tag{7}$$

We can use L_n to obtain the good probability of the path from curves as shown in Fig. 1 if the clock period is determined.

Based on the notion of conditional probability discussed in this section, testing the same set of longest paths will lead to higher fault coverage than that predicted in Table 2. We evaluated the fault coverages of the longest paths for ISCAS-85 benchmark circuits when conditional probability was taken into account. The fault coverages for the longest paths (ϕ_c) are listed in the 4th column in Table 3. It can be seen that the fault coverage

Table 3. Fault coverage evaluation using conditional probability.

Circuit	Longest paths	ϕ	ϕ_c
c432	4374	0.41	0.702
c499	3072	0.94	0.966
c880	108	0.37	0.698
c1355	196608	0.39	0.753
c1908	32	0.047	0.516
c2670	512	0.12	0.569
c3540	96	0.028	0.543
c5315	12	0.025	0.562
c6288	6.4×10^{10}	0.00041	—
c7522	7	0.025	0.438

results are much higher than the original results shown in Table 2 (repeated as the 3rd column in Table 3). Note that the circuit c6288 has an extremely large number of paths, and that many of the critical paths are not effectively conjoined with others. Choosing the right paths for such circuits is still difficult.

5. FAULT COVERAGE EVALUATION

In practice, a segment in the path under consideration may be conjoined with more than one tested good path. For example, consider a segment conjoined with two tested good paths, where these two good paths share only one common segment. Let $P(A)$ and $P(B)$ denote the good probability of the two paths, π_A and π_B , respectively, and let $P(A \wedge B)$ denote the probability when both π_A and π_B are good. Then the conditional probability function for the segment considered is

$$f(x|A \wedge B) = \frac{f(x)P(A \wedge B|x)}{P(A \wedge B)}. \quad (8)$$

If π_A and π_B have only one common segment, then $P(A \wedge B|x)$ can be simplified as

$$P(A \wedge B|x) = P(A/x)P(B/x). \quad (9)$$

Therefore,

$$\begin{aligned} f(x|A \wedge B) &= \frac{f(x)P(A|x)P(B|x)}{P(A)P(B|A)} \\ &= \frac{f(x|A)P(B|x)}{P(B|A)}. \end{aligned} \quad (10)$$

The mean delay of the segment under event A is $f(x/A) = \mu_c$. Therefore, $P(B/x) = P(B/A)$ if $x = \mu_c$. Note that the curves for $f(x/A)$ and $f(x|A \wedge B)$ intersect at $x = \mu_c$. Also, from (6), we know that $f(x|A \wedge B) > f(x/A)$ for $x < \mu_c$, and that $f(x|A \wedge B) < f(x/A)$ for $x > \mu_c$. Moreover, the distribution of $f(x|A \wedge B)$ is similar to that of $f(x/A)$ shifted to the left; i.e., the mean of $f(x|A \wedge B)$ is smaller than that of $f(x/A)$. Fig. 4 plots the modified probability functions for different numbers of conjoined paths with a single shared segment. More good conjoined paths sharing a segment will move the distribution and mean further to the left. Table 4 lists the resulting means and variances of the shared segment for different numbers of conjoined paths using the same example shown in Fig. 3.

If π_A and π_B share more than one common segment, then (9) can not be used since $P(A \wedge B|x)$ will be less than $P(A/x)P(B/x)$ in this case. In general,

$$P(A \wedge B|x) = P(A/x)P((B/A)|x). \quad (11)$$

Note that if there is only one shared segment between π_A and π_B , then $P((B/A)|x) = P(B/x)$. We can now obtain the general conditional probability function

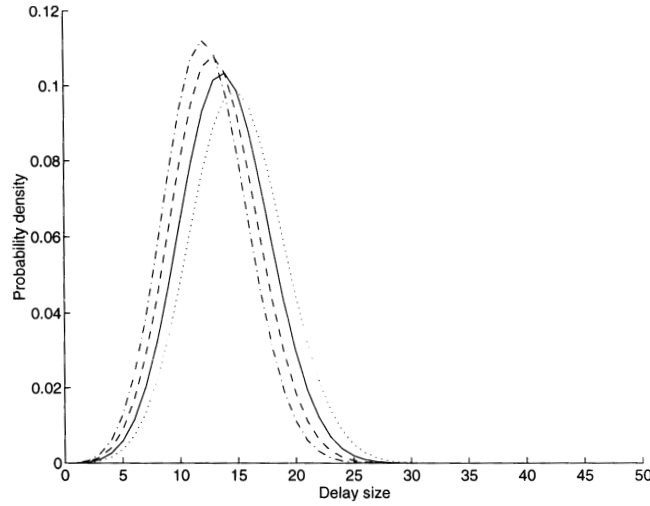


Fig. 4. Modified probability functions for two conjoined good paths (dashed) and three conjoined good paths (dot-dashed), as compared with those shown in the previous figure.

Table 4. The means and variances of the shared segment for different numbers of conjoined paths.

No. conjoined paths	0 (Original)	1	2	3
Mean	15	14.0	13.1	12.3
Variance	16	14.5	13.3	12.3

$$f(x|A \wedge B) = \frac{f(x|A)P((B|A)|x)}{P(B|A)} \tag{12}$$

If $x = \mu_c$, then $P((B|A)/x) = P(B|A)$. Therefore, $f(x|A \wedge B) = f(x|A)$ when $x = \mu_c$. In general, if a segment is shared by more tested good paths, the segment will have lower mean and variance for its delay size even if the paths have other shared segments.

Once the mean and variance for every segment are derived, we can use linear programming to obtain the good probability of every untested path. Then we can evaluate the fault coverage from the derived good probability of untested paths and carefully select the test set so as to improve the efficiency of path-delay fault testing.

6. CONCLUSIONS

A probabilistic model for delay fault testing has been proposed. Based on the correlation among the conjoined paths and the conditional probability analysis, the real delay size of an untested path has been shown to be less than its original (assumed) value if the

path is conjoined with other tested paths (which are known to be good). Conditional probability has been used to derive the new probability distribution of the delay size and to evaluate the effective fault coverage necessary for more effective path delay-fault testing, including better fault coverage evaluation and path selection.

The limitations of this work include: (1) effective application of this approach would depend on the availability of the delay distribution from the product line; (2) the complexity grows rapidly if multiple conjoined paths are considered; (3) only combinational circuits have been considered so far; and (4) false paths and untestable paths should be identified first, and delay-fault ATPG is still required. More investigations could be done to address these issues and to search for applications of this approach.

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