JOURNAL OF INFORMATION SCIENCE AND ENGINEERING 26, 585-595 (2010)

Low Parasitic Capacitance and Low-Power CMOS Capacitive Fingerprint Sensor*

MENG-LIEH SHEU, WEI-HUNG HSU AND YUAN-CHANG HUANG
Department of Electrical Engineering
National Chi Nan University
Puli, Nantou, 545 Taiwan

In this paper, a low parasitic capacitance and low-power CMOS capacitive fingerprint sensor readout circuit is presented. The side effect of parasitic capacitance has been under control with novel layout structure in sensor cell, and minimal size switch is used to reduce non-ideal effects of MOS switch and achieve good linearity. Power dissipation is also reduced with quiescent current control in buffer amplifier of sensor cell. A prototype chip with 32 × 32 array size has been fabricated using TSMC 0.35μm CMOS process. The chip works at 3.3V power supply and operates at 4MHz clock rate. Capacitance value from 0fF to 60fF can be sensed, corresponding analog output voltage is from 3.02V to 1.57V and the digital output is 6 bits. The overall power consumption is less than 5.5mW.

Keywords: biometric technology**,** fingerprint sensor, low-power, capacitive sensing, SAR ADC

1. INTRODUCTION

Nowadays the convenience of mobile appliances like IC cards, notebook computers and cellular phones brings us better life but also into the privacy threat. The more widespread these mobile appliances are, the more significant the issue on personal security is. The demand for user authentication is becoming more and more important. Conventional protection schemes such as personal identification number (PIN) or password are no longer competent and could be replaced by biometric technology. Some biometrics have been popularly applied in authentication such as: fingerprint, hand geometry, iris, and voice print [1]. Because of the property of low-cost, easy integration and high reliability, many researches have been reported on fingerprint acquisition.

Fingerprint acquisition can be performed by capacitive sensing scheme [2-7]. To distinguish the variations of the electrical field established between the fingertip's skin and the sensor plate is the origin of the design concept for a readout circuit for the capacitive fingerprint sensors. To our objective, a readout circuit for capacitive fingerprint sensor should satisfy the requirements of low power, high sensitivity and wide output dynamic range [8]. Recent works [3, 6] have shown that, by applying capacitive sensing scheme, the fingerprint sensor and its readout circuit can be easily integrated in standard CMOS process. However, parasitic capacitance nearby the fingerprint sensor usually reduces the sensitivity and the output dynamic range, which makes the design of the read-

Received March 18, 2008; revised July 14, 2008; accepted August 28, 2008.
Communicated by Liang-Gee Chen.
* This work has been partially supported by the National Science Council of Taiwan, R.O.C., under grant No. NSC 96-2221-E-260-027. The authors would like to thank Chip Implementation Center (CIC) for the help on chip fabrication.

out circuit complicated. Besides, to equip the fingerprint acquisition device within mobile devices, low power consumption should be an important concern.

In the following content, we will propose a capacitive sensing scheme which is insensitive to parasitic capacitance and suitable for fingerprint acquisition. In our proposed scheme, the parasitic capacitance (C_s) is formed under the control by the area of the top layer as the sensing plate and the second layer as the coupling plate. The residue parasitic capacitance (C_p) induced from the coupling plate to the substrate can be considered as little influence through charge balance during our capacitive sensing scheme. A wide dynamic range with almost half of the V_{DD} voltage is obtained by the charge redistribution method. In addition, the sensor and its readout circuit are designed in the same chip by using standard CMOS process. A prototype fingerprint sensor chip is realized by a 32 × 32 sensor array with peripheral control logic and an analog to digital converter (ADC). A quiescent current control switch is placed in each pixel cell of the array to reduce static power consumption. In the next section, the operation of fingerprint acquisition will be presented. In section 3, we will discuss the detail of the circuit architecture. Finally, the measurement results and conclusions will be stated in sections 4 and 5, respectively.

2. FINGERPRINT SENSOR STRUCTURE

2.1 Capacitive Fingerprint Sensor

Fingerprint sensor depending on capacitive sensing scheme is generally constructed as Fig. 1. In microscopic scale, the surface on the finger may have deeper part like valley or more elevated like ridge. In standard CMOS process the top metal can be exploited as the fingerprint sensor plate where the area of the sensor plate is denoted as A. As the fingertip surface approaching the sensor plate, capacitance can be induced according to two factors: dielectric constant (ε_x) and the distance between the surface and the sensor plate (d_x). The induced capacitance, C_f, can be expressed as:

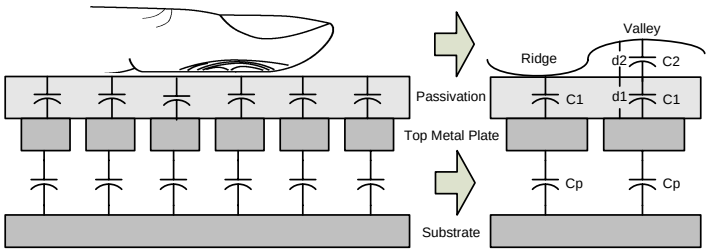


Fig. 1. Capacitive fingerprint sensor.

$$C_f = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}, \tag{1}$$

where C_1 ($C_1 = A\varepsilon_1/d_1$) is a larger capacitance induced by the ridge part of fingerprint,

while the valley part will produce a much smaller capacitance of C_2 ($C_2 = A\varepsilon_2/d_2$) in series with C_1. According to the parameters of standard CMOS process and required resolution, a pixel size of about 50μm × 50μm to achieve 500 pixels per inch well suitable for fingerprint image acquisition, hence a reasonable estimation on the induced capacitance is ranged from 0 to 60 fF. By measuring how large C_f is, we can distinguish where the valley or the ridge is. Notice that C_P is the parasitic capacitance formed by metal plate to substrate.

2.2 Capacitive Sensing Scheme

The induced capacitance, C_f, has to be transformed to voltage or current for subsequent signal processing. The capacitive sensing scheme can be setup as in Fig. 2. The output voltage, V_{OUT}, can carry the information of what C_f changes. First of all, the sensing plate is connected to V_1 in phase ϕ_1; meanwhile, the coupling plate is connected to substrate. In phase ϕ_2, the sensing plate is kept open while the coupling plate is connected to V_2. Then the net charge on V_{OUT} after charge redistribution in phase ϕ_1 and ϕ_2 can be respectively written as:

$$Q = V_1(C_f + C_s) = V_{OUT} \cdot C_f + (V_{OUT} - V_2)C_s. \tag{2}$$

The short circuit on C_p in phase ϕ_1 force the net charge on C_p equal to zero. Rearrange Eq. (2), the V_{OUT} due to capacitive sensing scheme can be expressed as:

$$V_{OUT=}V_1 + V_2\left(\frac{C_s}{C_f + C_s}\right). \tag{3}$$

Therefore, by measuring the variation of V_{OUT}, the ridge and valley on the fingerprint can be found.

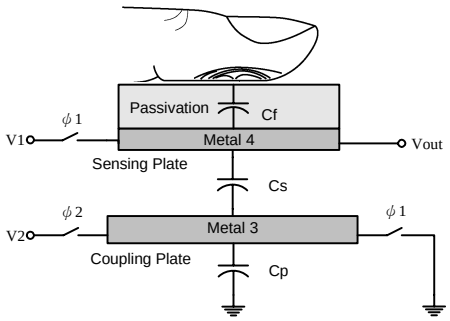


Fig. 2. Capacitive sensing scheme.

2.3 Non-ideal Effect

Fig. 3 shows the realization of capacitive sensing scheme by MOSFET transistors, which are labeled by MP1, MN2, and MN1. Besides, the parasitic capacitances from

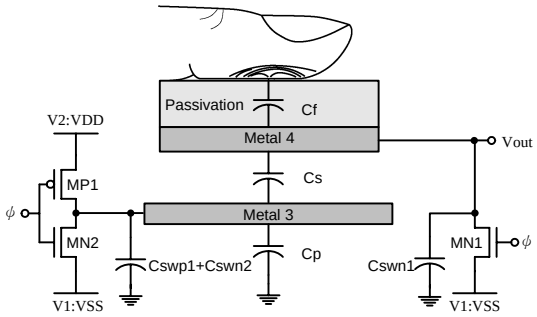


Fig. 3. Capacitive sensing scheme constructed by MOSFET transistors.

switches are C_{swn1}, C_{swp1} and C_{swn2}. To obtain the widest dynamic range, V_2 is set by V_{DD} and V_1 is set by ground (V_{SS}). Different from Fig. 2, the control signal is simplified into single phase, ϕ. Because the non-ideal effects result from parasitic capacitors, the V_{OUT} of Eq. (3) is modified to be:

$$V_{OUT} = V_1' + V_2' \left(\frac{C_s}{C_f + C_s + C_{swn1}} \right), \tag{4}$$

where V_1' and V_2' are the voltages which V_1 and V_2 passes through MOS switches. The major non-ideal effects due to MOS switches are charge injection and clock feedthrough. V_1' and V_2' can be expressed as:

$$V_1' = V_1 - K_1 \left(\frac{C_{ox}(V_{GS1} - V_{THN1})}{2(C_P + C_s + C_{swn1})} \right), \tag{5}$$

$$\begin{aligned} V_2' = V_2 &- \left[(V_{DD} - V_{SS}) \left(\frac{C_{ov}}{C_{ov} + C_P + C_S + C_{swn2} + C_{swp1}} \right) \right] \\ &- K_2 \left(\frac{C_{ox}(V_{GS2} - V_{THN2})}{2(C_P + C_s + C_{swn2} + C_{swp1})} \right), \end{aligned} \tag{6}$$

where C_{ox} is the capacitance per unit area of the gate oxide, V_{THN} is the threshold voltage, C_{ov} is the overlap capacitance owing to MOSFETs structure, $K_{1,2}$ is the modification coefficient for charge-injection formulation. Put Eqs. (4), (5) and (6) together to observe the non-ideal error, we can find out the non-ideal error will be proportional to the area of MOS switches. However, minimum MOS switches may result in pessimistic process variations to degrade the reliability of the sensor array. In such case, we adopt unit transistor size to reduce non-ideal error and keep process variations under control.

Fig. 4 shows the complete schematic of a unit pixel. All the MOS switch size is set to 0.7μm/0.35μm. A unity gain buffer can isolate the routing parasitic capacitance from the readout circuit. To effectively reduce static power consumption, the operation current of the unity gain buffer is supplied by a power gate, MP3. Only the chosen pixel can turn on the power gate during fingerprint sensing; otherwise, the power gate is cut-off.

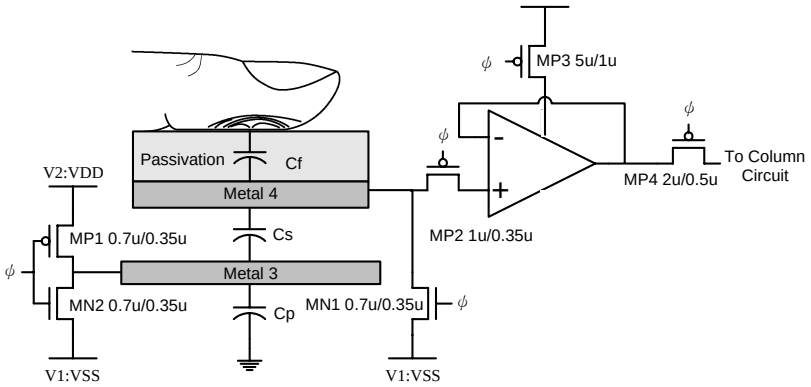


Fig. 4. The complete schematic of a unit pixel.

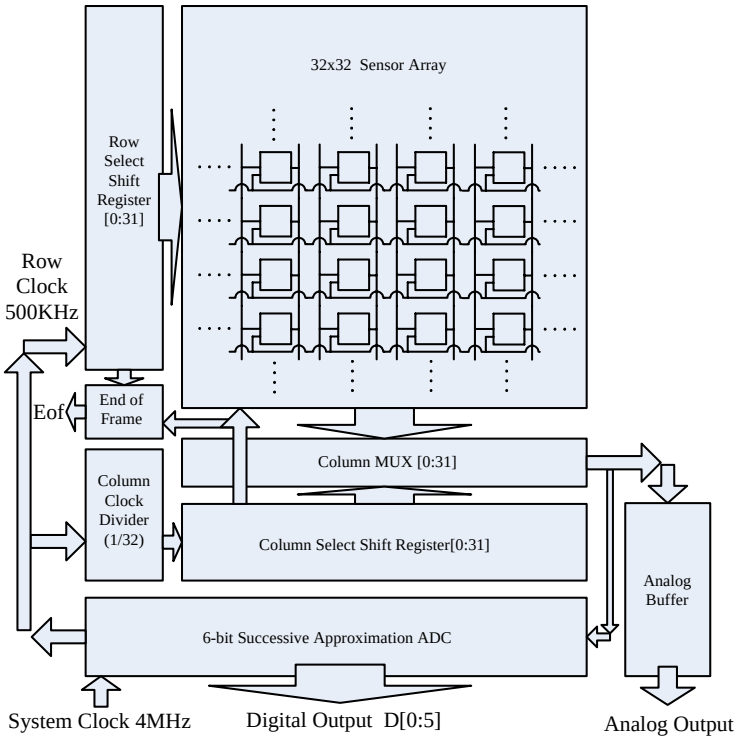


Fig. 5. The architecture of the 32 × 32 sensor array.

3. 32 × 32 SENSOR ARRAY CHIP IMPLEMENTATION

To verify the proposed capacitive sensing and low power control schemes, a prototype chip is designed and implemented using TSMC 0.35μm CMOS process. The architecture of the 32 × 32 sensor array is shown in Fig. 5. To simplify the reading procedure, pixel-wise scanning is adopted to acquire the fingerprint data one pixel at a time. Row

and column select shift registers accomplish the above scanning. Through the column multiplexer (column MUX), the read output voltage can be sent to a 6-bit successive approximation register (SAR) ADC to be transformed to digital data. The 6-bit SAR ADC uses 4MHz clock to convert read output voltage. After one complete scan of the array, an end-of-frame (Eof) signal will be generated at the end of a frame block.

To observe the effect of parasitic capacitance of MOS switches, three kinds of MOS switch size are simulated. The transfer curves are depicted in Fig. 6. As discussed in section 2, the ideal switch can produce the widest dynamic range. Using minimal size switches, the transfer curve is nearly close to the ideal one. With the size of MOS switches increasing, the dynamic range also decreases. To verify the effect resulting from the non-uniform distribution of circuit parameters, Monte Carlo simulations are performed with the size of switches and unity gain buffer, and the coupling capacitance set by 10% variation in Gaussian distribution. After Monte Carlo simulations, output voltage fluctuating about 90mV and 60mV are observed under C_f = 60fF and 0fF, respectively.

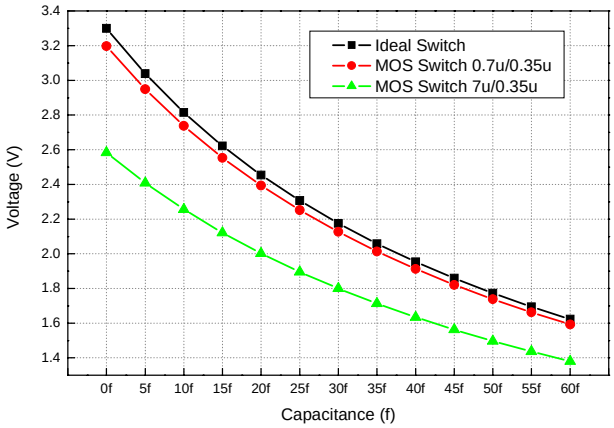


Fig. 6. Comparison of different sizes of MOS switches.

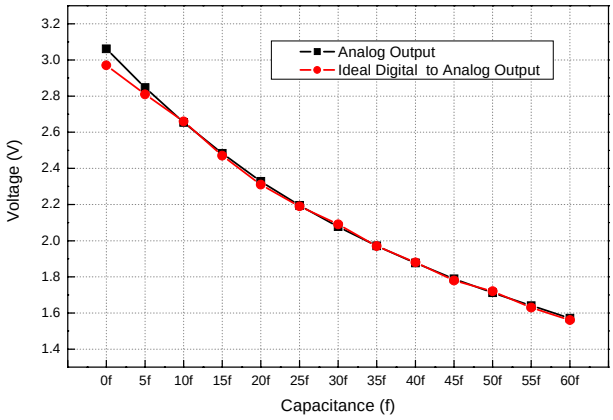


Fig. 7. Simulation result of output voltage versus fingerprint capacitance.

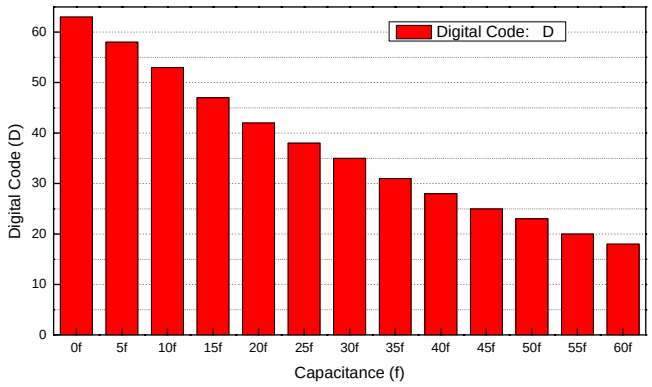


Fig. 8. Simulation results of the 6-bit ADC.

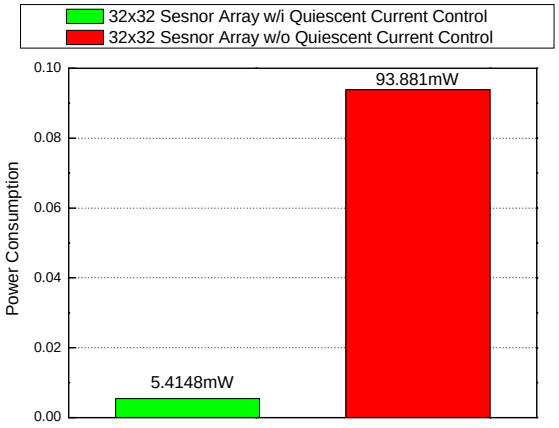


Fig. 9. The reduction of power consumption.

Fig. 7 shows the simulation result of the transfer curve of sensing capacitance to voltage of unit pixel. The output is ranged from 3.1V to 1.6V for capacitance varied from 0fF to 60fF. Through applying an ideal digital to analog converter (DAC), the digital data from the 6-bit SAR ADC can be reconverted to the analog voltage. A difference can be found only around 0fF capacitance. The simulated digital code of the 6-bit SAR ADC is recorded in Fig. 8. It ranges from 63 to 18 for from voltage varied from 3.1V to 1.6V. The effect of power gate can be found in Fig. 9. The adoption of power gate can stop wasting quiescent current on non-sensed pixels. Each time only one pixel is sensing while the other pixels are idling and power off. The power consumption hence is mainly coming from the peripheral and ADC circuits.

4. MEASUREMENT RESULTS

The photograph of fabricated chip is shown in Fig. 10. The measured Eof signal shown in Fig. 11 guarantees that the peripheral control logic functions well. Fig. 12 shows a measuring waveform on a real finger, where the upper waveform is the sensed analog

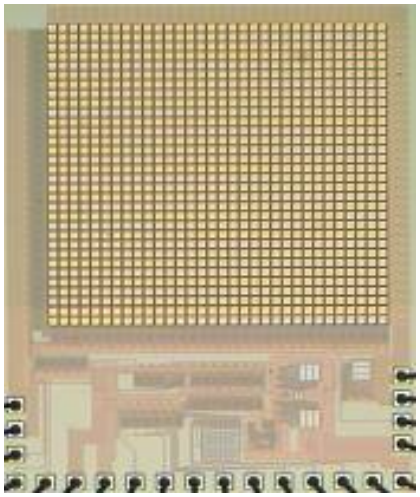


Fig. 10. The chip photograph.

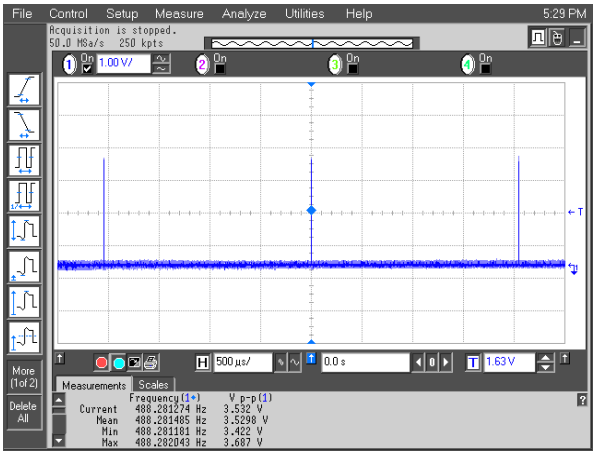


Fig. 11. The measured Eof signal.

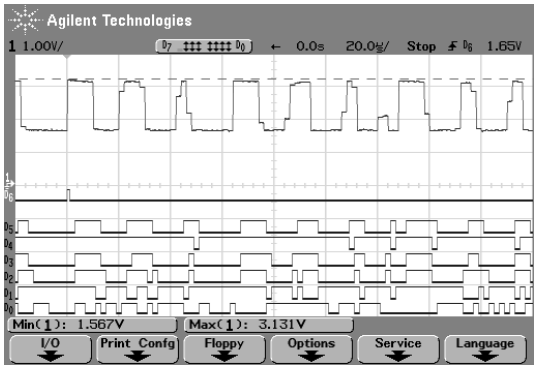


Fig. 12. The measured waveforms of a fingerprint.

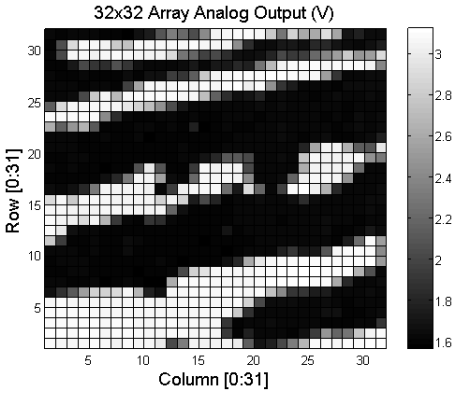


Fig. 13. The image constructed from analog output.

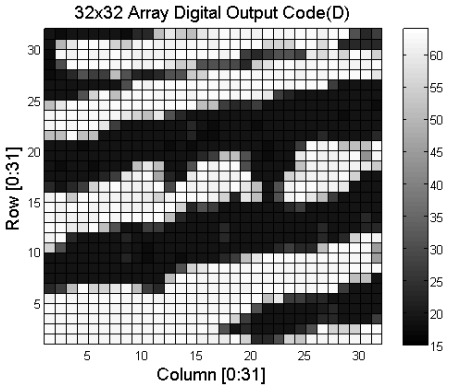


Fig. 14. The image constructed from the ADC output data.

signal and the lower waveforms are the 6-bit digital output. The measurement result is ranged from 3.11V to 1.57V, which is very close to the simulation result ranged from 3.1V to 1.6V. Figs. 13 and 14 show the images constructed from the sensed analog output and converted digital output codes, respectively. The valleys and ridges of the fingerprint can be clearly differentiated. The measured power consumption is less than 5mW.

5. CONCLUSIONS

The proposed capacitive sensing scheme has been successfully verified by a 32 × 32 sensor array prototype chip fabricated by using TSMC 0.35μm CMOS standard process. The measurement and simulation results are well matched. The characteristics of the fabricated fingerprint sensor chip are summarized in Table 1. Non-ideal effect has been investigated by Monte Carlo simulations. The modeling and calculations of non-ideal errors can provide good suggestions on MOS switches size.

Table 1. Chip summary.

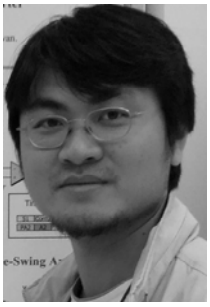
Process	TSMC 0.35μm
Power Supply	3.3V
Clock	4MHz
Array Size	32 × 32
Pixel Area	50 × 50μm^2
Capacitance	60fF ~ 0fF
Analog Output	1.57V ~ 3.02V
Digital Output	63 ~ 18（6-bit）
Power Consumption	＜5.5mW

REFERENCES

1. A. Jain, *et al*., *Biometrics Personal Identification in Networked Society*, Kluwer Academic Publishers, Norwell, MA, 1999.

2. J. W. Lee, *et al.*, "A 600-dpi capacitive fingerprint sensor chip and image-synthesis technique," *IEEE Journal of Solid State Circuits*, Vol. 34, 1999, pp. 469-475.
3. K. H. Lee and E. Yoon, "A 500 dpi capacitive-type CMOS fingerprint sensor with pixel-level adaptive image enhancement scheme," *ISSCC Digest of Technical Papers*, Vol. 2, 2002, pp. 282-283.
4. M. L. Sheu, C. K. Lai, W. H. Hsu, and H. M. Yang, "A novel capacitive sensing scheme for fingerprint acquisition," in *Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits*, 2005, pp. 627-630.
5. S. J. Kim, K. H. Lee, S. W. Han, and E. Yoon, "A 200 × 160 pixel CMOS fingerprint recognition SOC with adaptable column-parallel processors," *ISSCC Digest of Technical Papers*, Vol. 1, 2005, pp. 250-596.
6. S. M. Jung, J. M. Nam, D. H. Yang, and M. K. Lee, "A CMOS integrated capacitive fingerprint sensor with 32-bit RISC microcontroller," *IEEE Journal of Solid-State Circuits*, Vol. 40, 2005, pp. 1745-1750.
7. M. L. Sheu, Y. S. Tiao, W. F. Yang, and H. M. Yang, "A sweeping mode CMOS capacitive fingerprint sensor chip," in *Proceedings of International Computer Symposiums*, 2006, pp. 250-596.
8. H. Morimura, S. Shigematsu, and K. Machida, "A novel sensor cell architecture and sensing circuit scheme for capacitive fingerprint sensors," *IEEE Journal of Solid-State Circuits*, Vol. 35, 2000, pp. 724-731.

Meng-Lieh Sheu (許孟烈) received the B.S. and M.S. degrees in Electronics Engineering from National Chiao Tung University, in 1984 and 1986, respectively. From 1986 to 1989, he served as an instructor at the Electronics Engineering Department of Chung-Hwa Junior College, Taipei. Then he was back to National Chiao Tung University and earned a Ph.D. degree in Electrical Engineering and Computer Science in 1995. From 1995 to 2000, he worked as an associate researcher at Chip Implementation Center (CIC) of National Science Council, and became the deputy director of chip implementation division in 1999. In August 2000, a year after the catastrophic earthquake, he joined the National Chi Nan University, Puli, Nantou, as an Associate Professor of Electrical Engineering Department. Since August 2008, he has also been the Chairman of Graduate Institute of Communication Engineering. His current area of interest includes VLSI design and test, sensor readout, mixed-signal and communication IC designs.



Wei-Hung Hsu (徐偉宏) received the B.S. degree in Electrical Engineering from National Chi Nan University, Puli, Nantou, in 2002; and he received the M.S. degree in Electrical Engineering from National Cheng Kung University, Tainan, in 2004. He is now pursuing Ph.D. degree in Electrical Engineering at National Chi Nan University, Puli, Nantou. His technical interests are in front-end circuit design of capacitive sensors and low-power analog circuit design.

Yuan-Chang Huang (黃元展) received the B.S. and M.S. degrees in Electrical Engineering from National Chi Nan University, Puli, Nantou, in 2005 and 2007, respectively. He is now working as an engineer of Analog & Memory Circuit Design Department in the ELAN Microelectronics Corporation, Hsinchu.