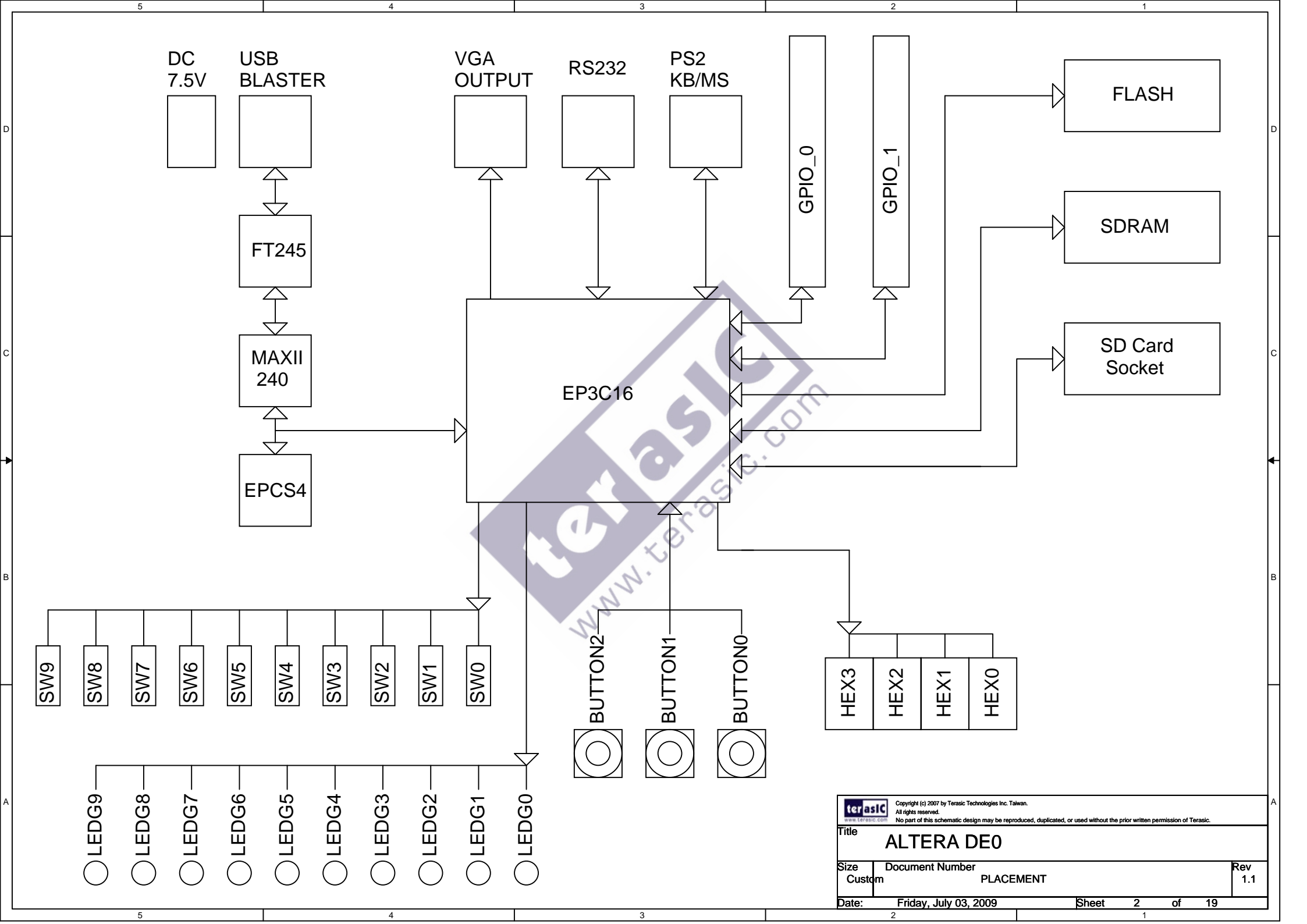



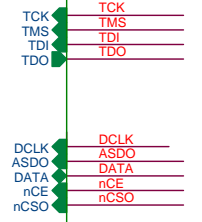
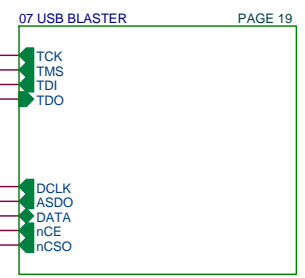
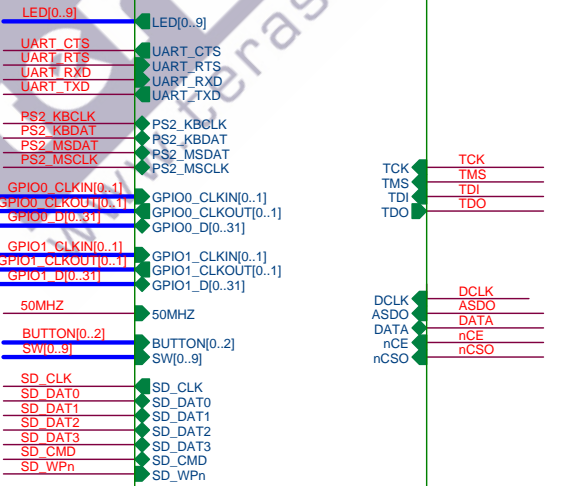
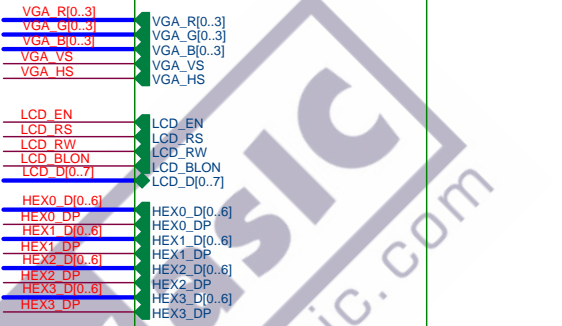
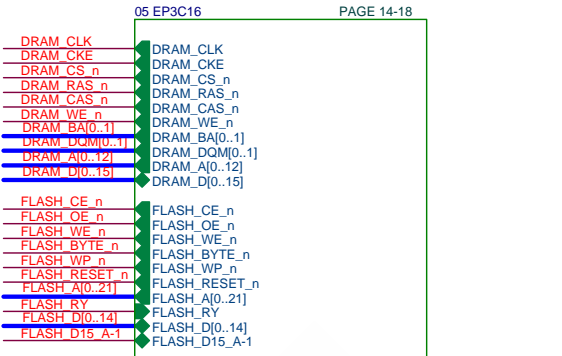
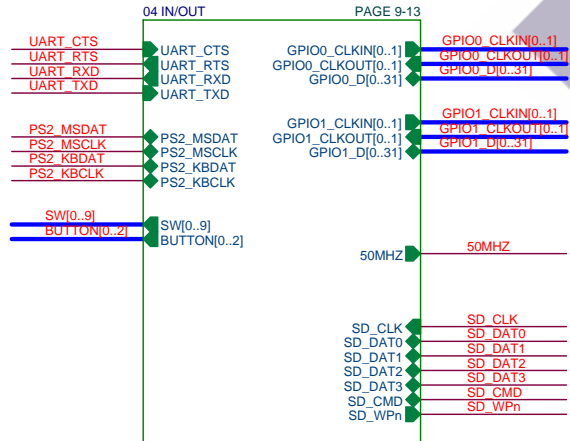
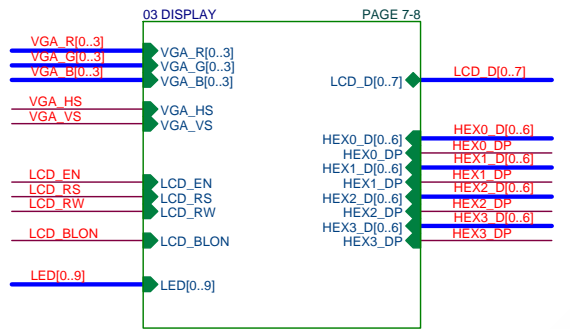
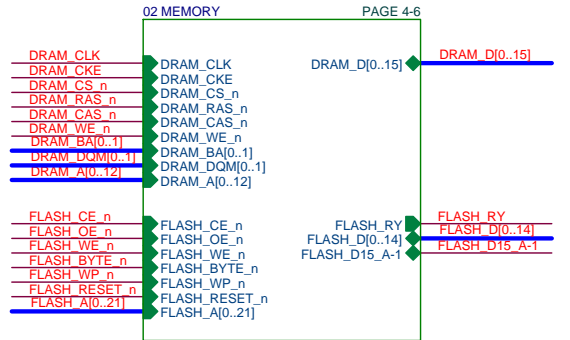
ALTERA CYCLONE III EP3C16 Development & Education BOARD

SCHEMATIC	CONTENT	PAGE
TOP	COVER PAGE, TOP	01 ~ 03
MEMORY	SDRAM,FLASH	04 ~ 05
DISPLAY	VGA, LED, 7SEGMENT	06 ~ 07
IN/OUT	CLOCK, PS2, RS232, BUTTON, SWITCH, CONNECTOR,SD CARD	08 ~ 12
FPGA	Cyclone II EP3C16 BANK1..BANK8 , POWER , CONFIG	13 ~ 17
POWER	POWER 1.2V,2.5V, 3.3V, 5V	18 ~ 18
USB BLASTER	USB BLASTER	19 ~ 19

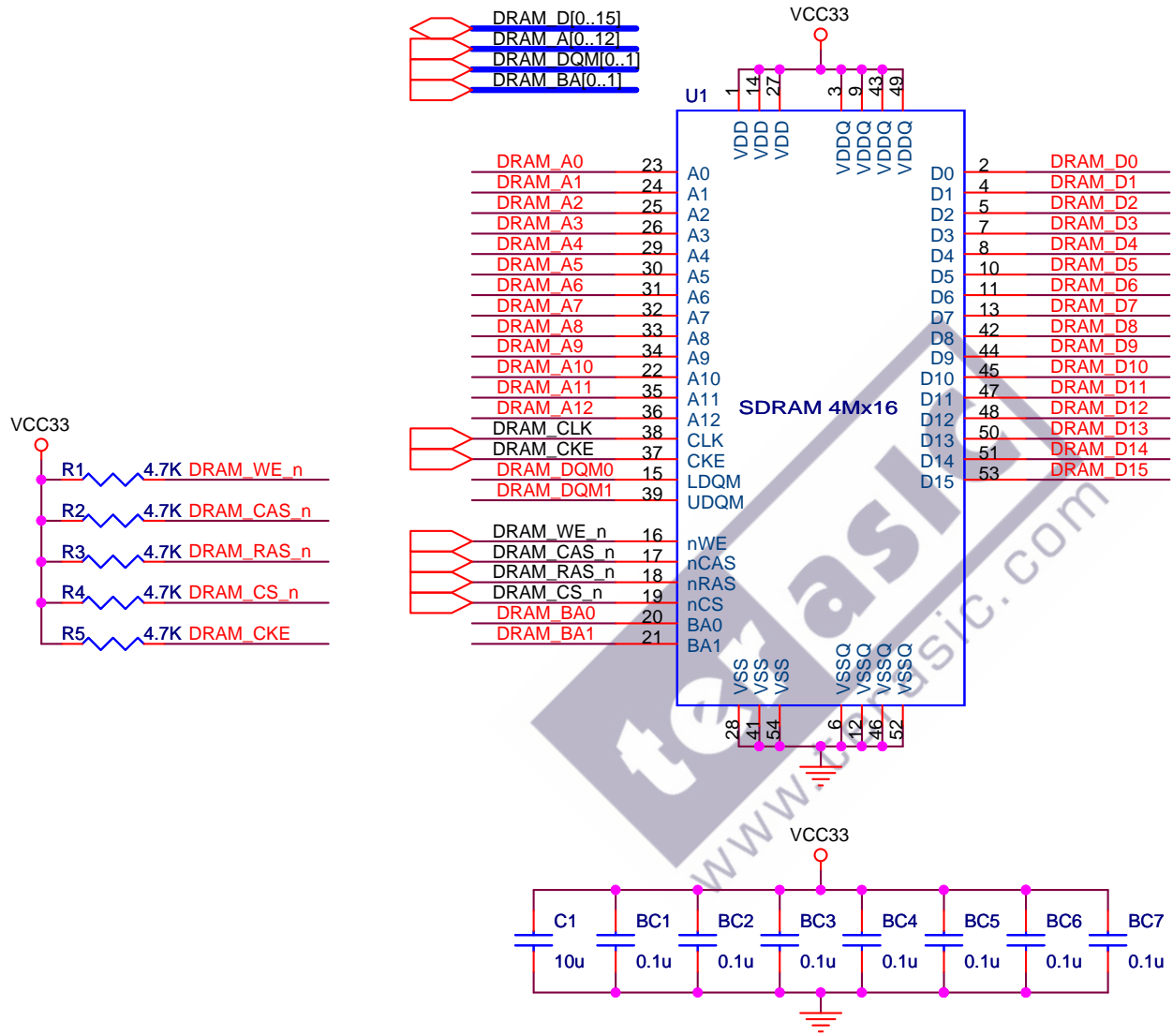





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Title		
ALTERA DE0		
Size	Document Number	Rev
Custom	PLACEMENT	1.1
Date:	Friday, July 03, 2009	Sheet 2 of 19

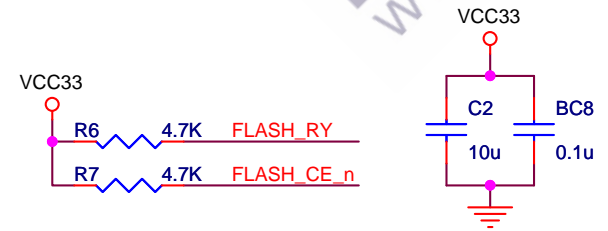
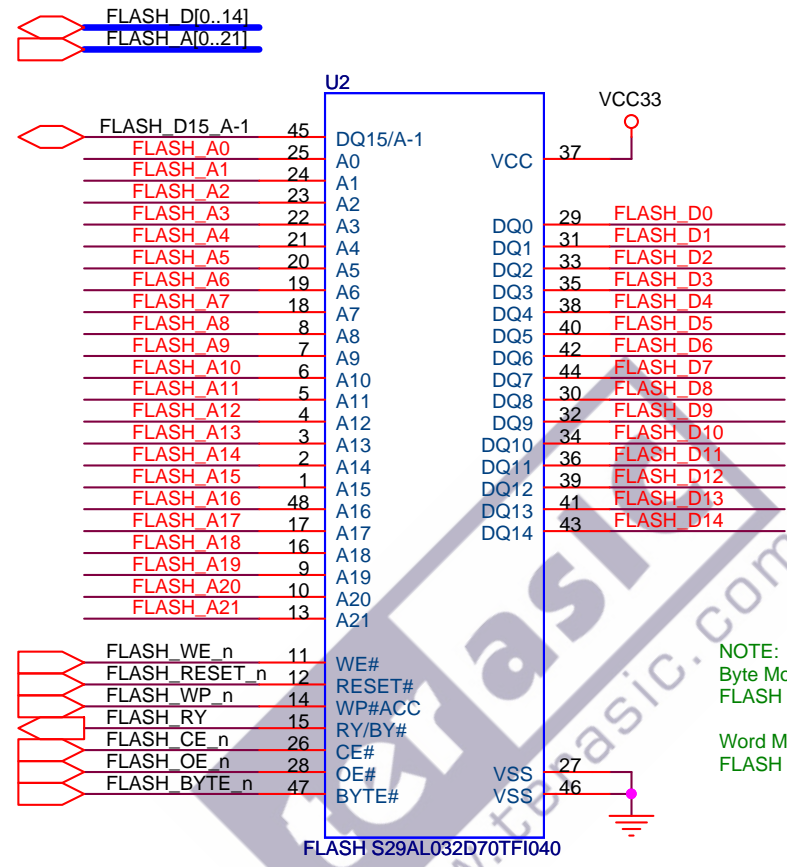



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Title ALTERA DE0	
Size B	Document Number TOP LEVEL
Date: Friday, July 03, 2009	Rev 1.1
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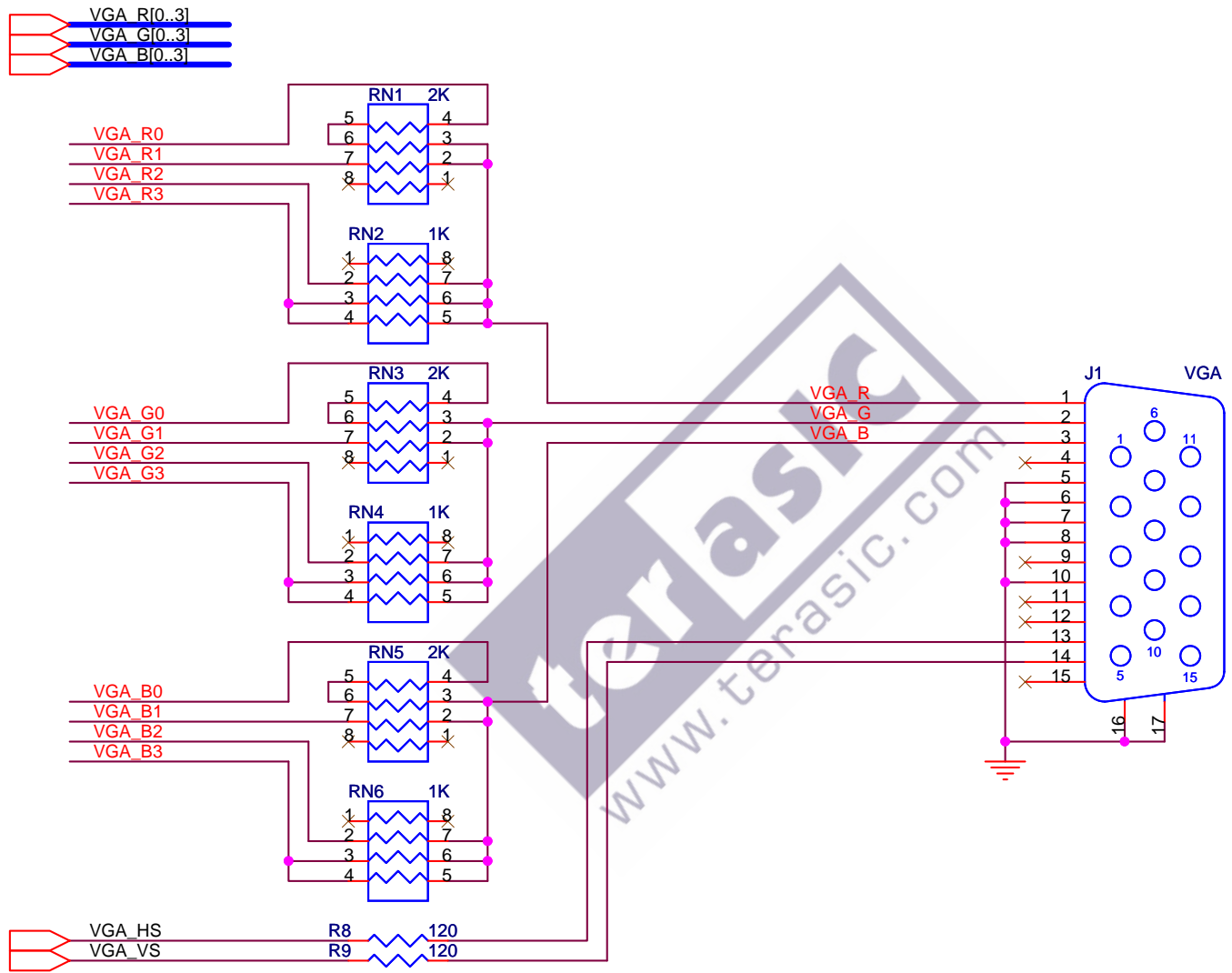



NOTE:
 SDRAM 4Mx16 (Default)
 SDRAM 8Mx16
 SDRAM 16Mx16
 SDRAM 32Mx16

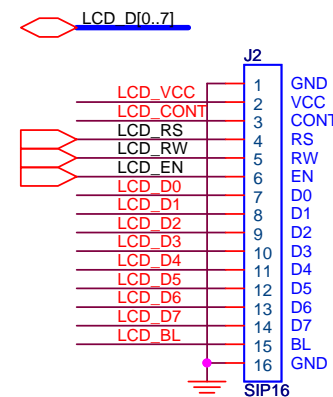
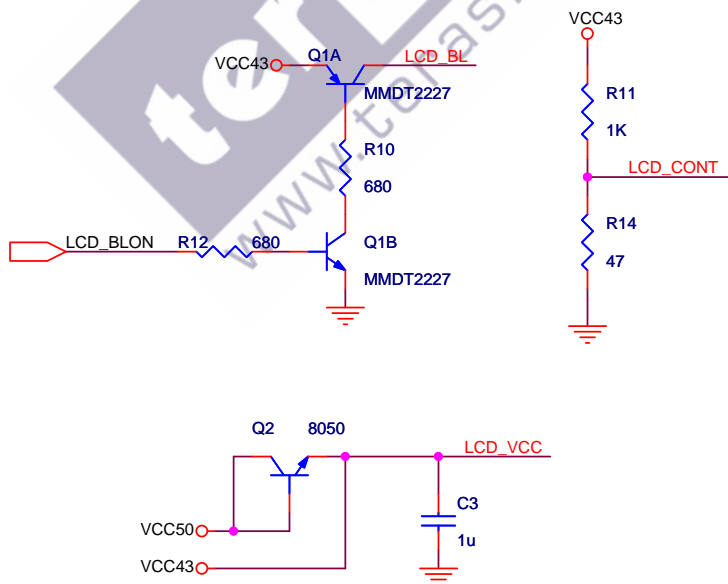
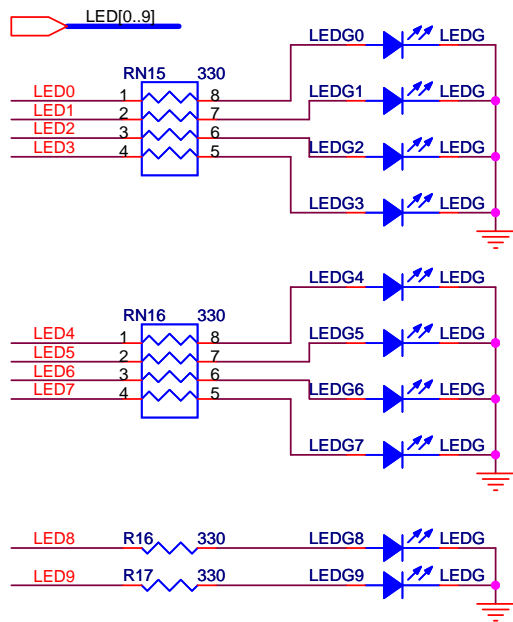
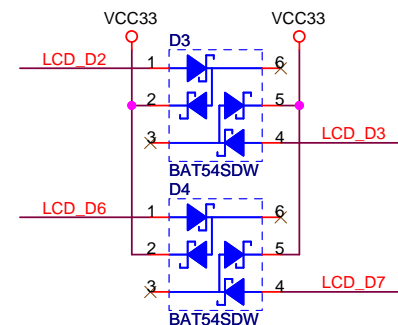
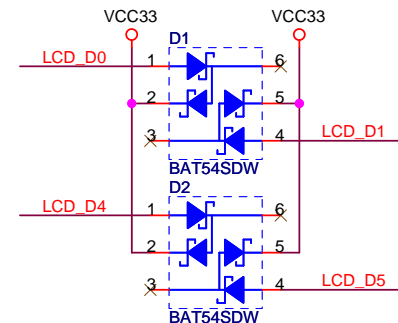
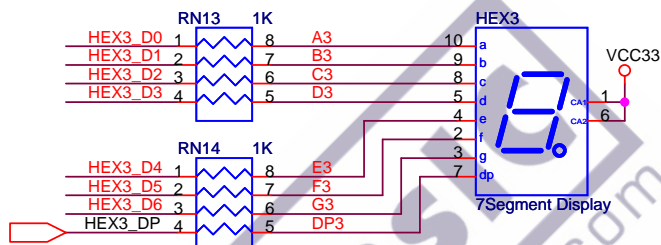
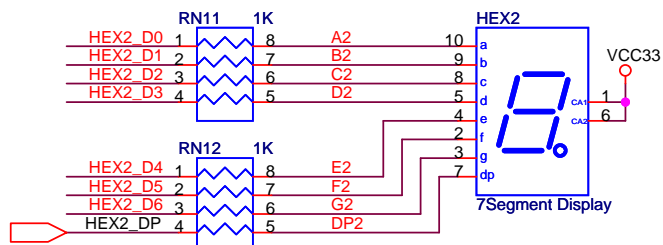
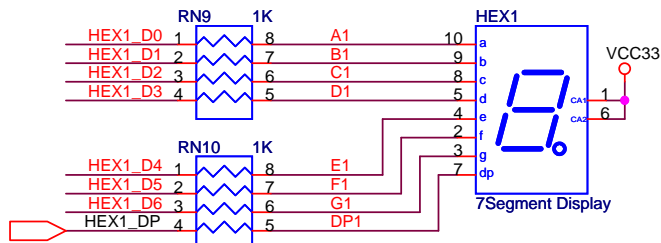
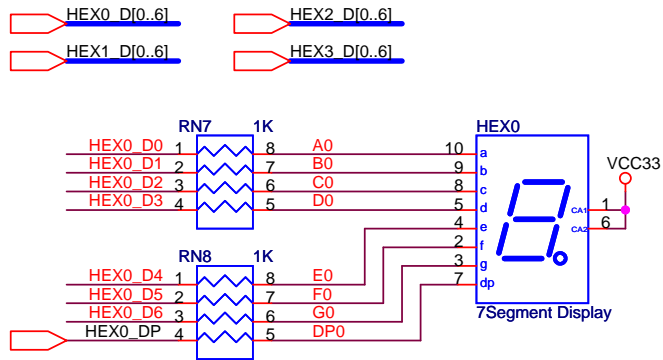
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Title		
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Size	Document Number	Rev
A	SDRAM	1.1
Date:	Friday, July 03, 2009	Sheet 4 of 19

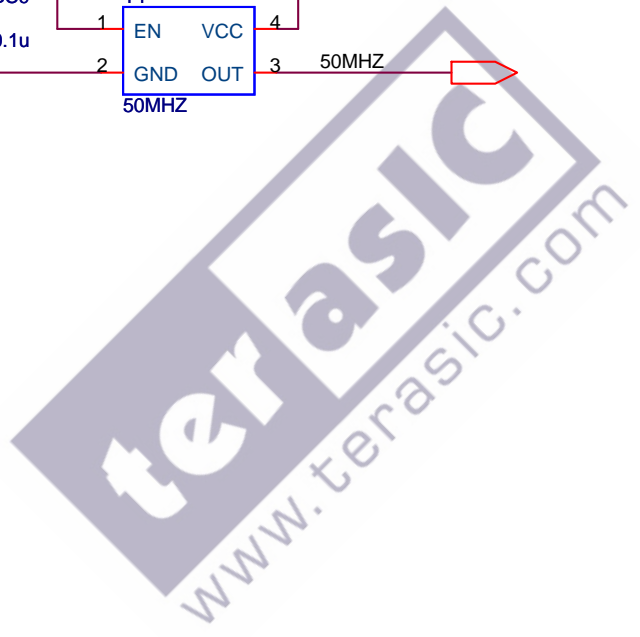
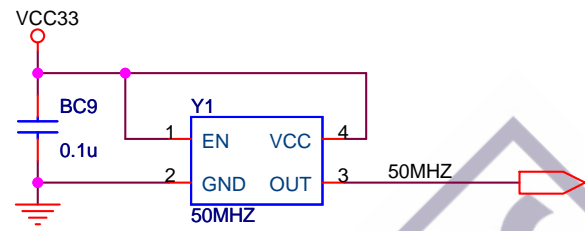



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Title		
ALTEA DE0		
Size	Document Number	Rev
A	FLASH	1.1
Date:	Friday, July 03, 2009	Sheet 5 of 19

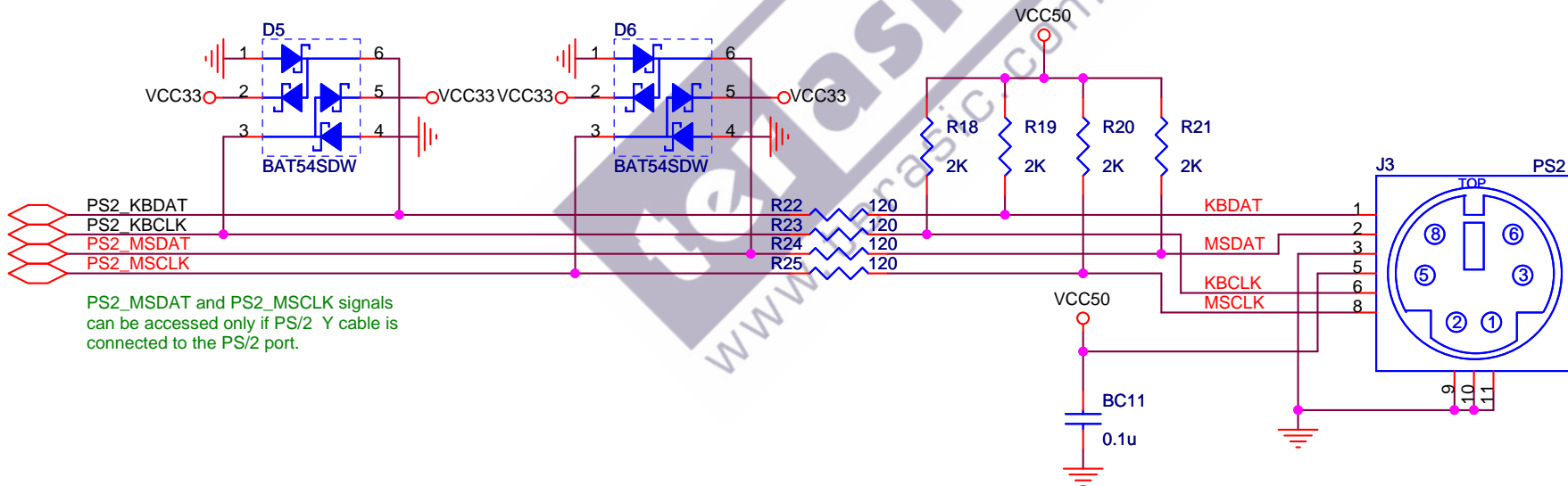
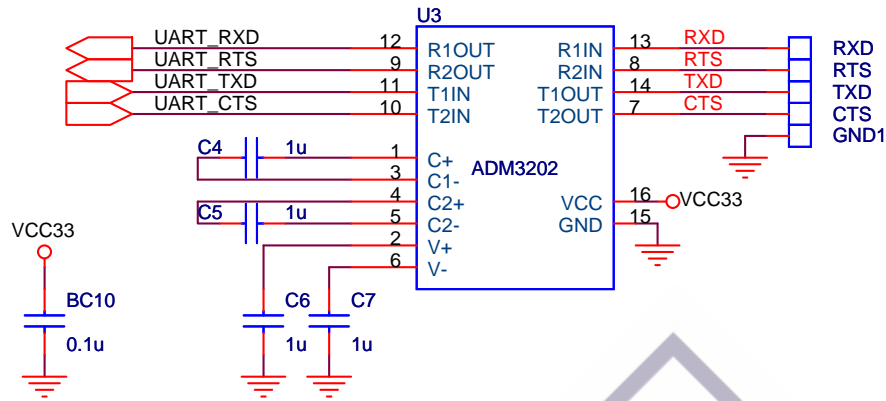



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Title		
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Size	Document Number	Rev
A	4 bit VGA Output	1.1
Date:	Friday, July 03, 2009	Sheet 6 of 19

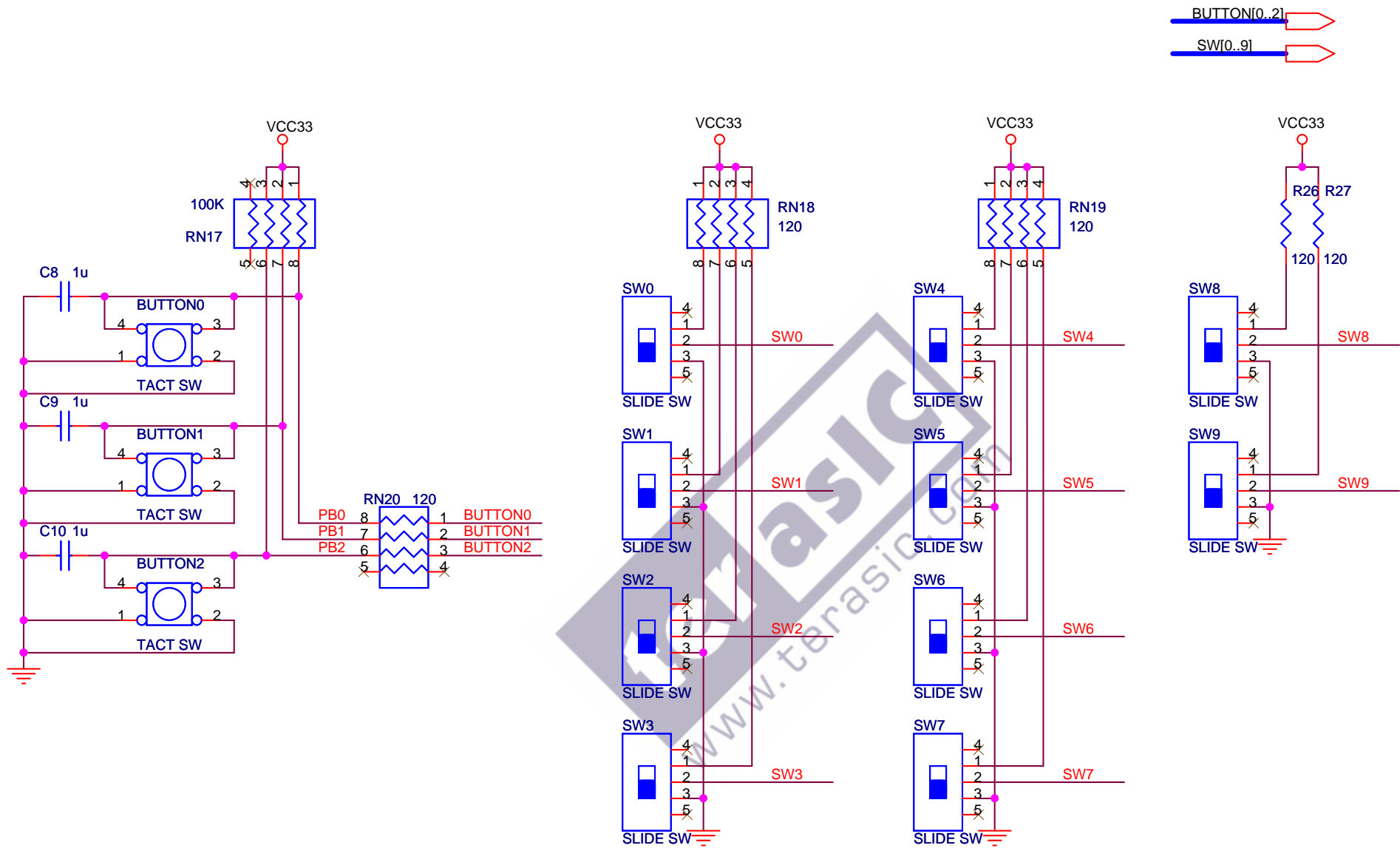





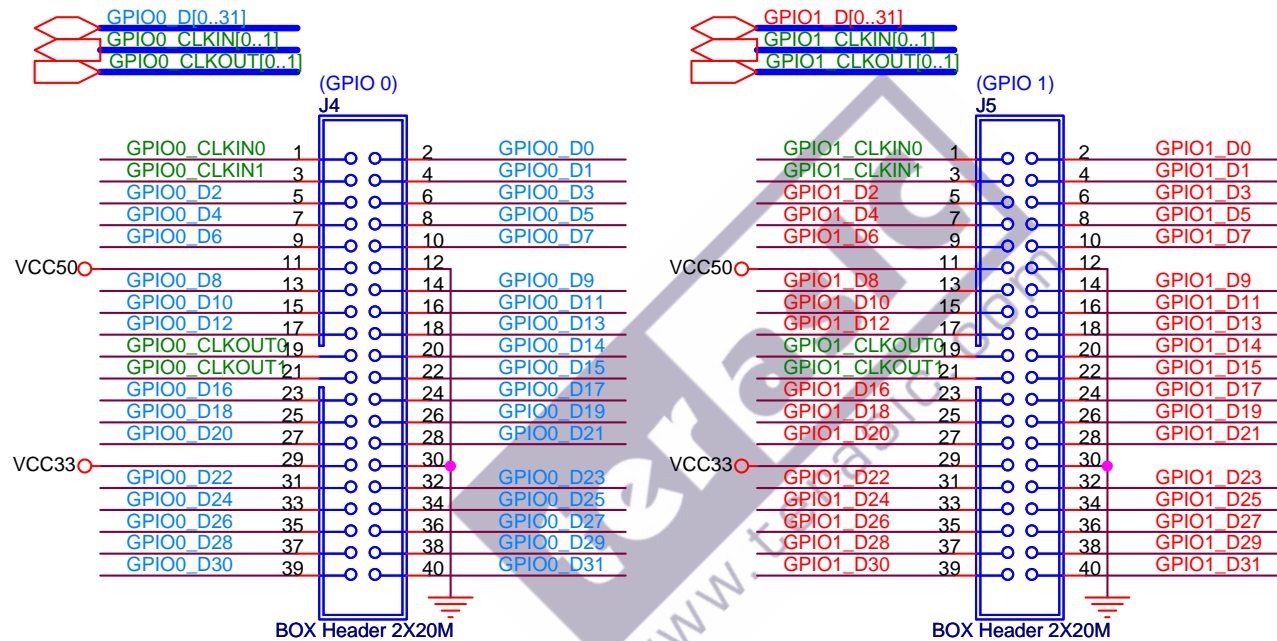
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Title ALTERA DE0		
Size A	Document Number CLOCK	Rev 1.1
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Title		
ALTERA DE0		
Size	Document Number	Rev
A	PS2 AND RS232	1.1
Date:	Friday, July 03, 2009	Sheet 9 of 19

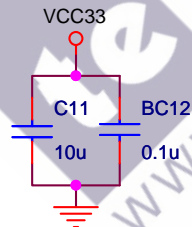
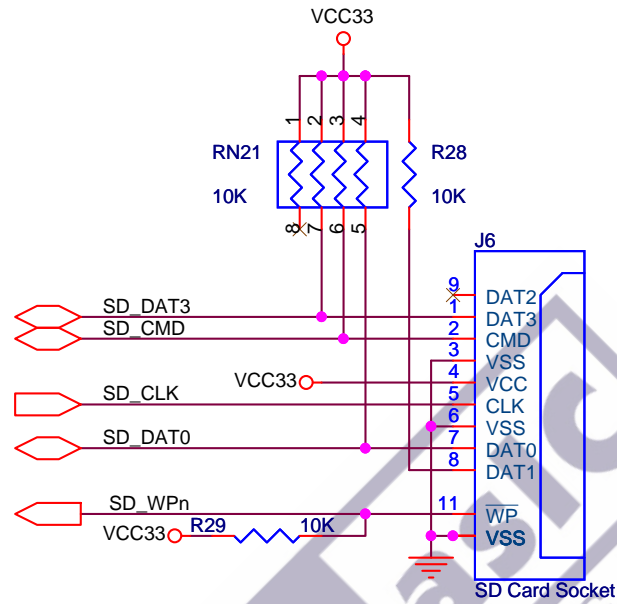



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Title		
ALTERA DEO		
Size	Document Number	Rev
A	Button and Switch	1.1
Date:	Friday, July 03, 2009	Sheet 10 of 19

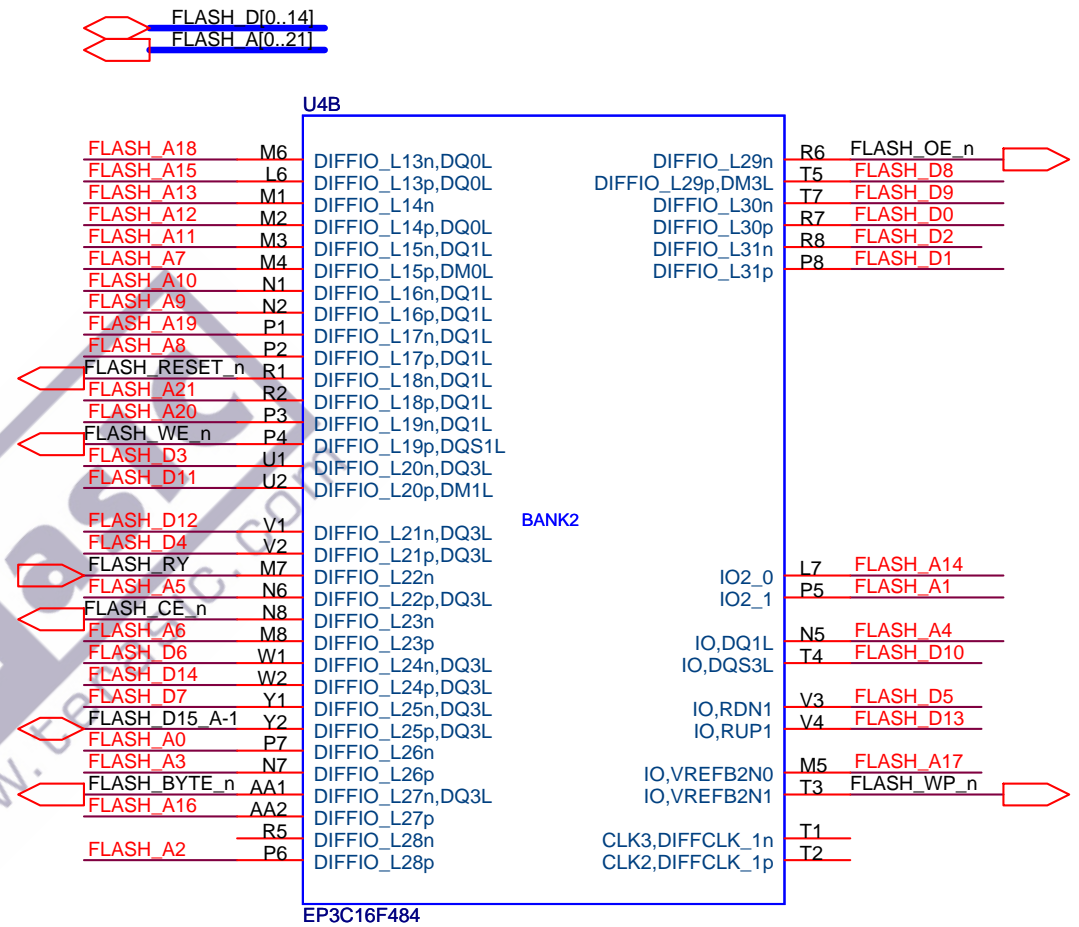
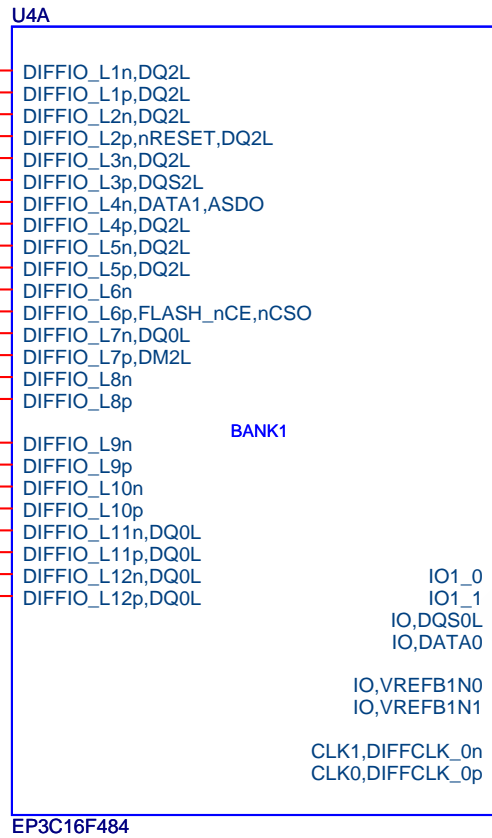



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Title		
ALTERA DEO		
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A	CONNECT	1.1
Date:	Friday, July 03, 2009	Sheet 11 of 19



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Title ALTERA DE0		
Size A	Document Number SD Card Socket	Rev 1.1
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Title **ALTERA DE0**

Size Custom Document Number **BANK1, BANK2** Rev 1.1

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GPIO0_D[0..31]
GPIO0_CLKIN[0..1]
GPIO0_CLKOUT[0..1]

GPIO1_D[0..31]
GPIO1_CLKIN[0..1]
GPIO1_CLKOUT[0..1]

U4C

GPIO0_D26	T8	DIFFIO_B1n	DIFFIO_B17n,DQ5B	W10	GPIO0_D25
GPIO1_D27	R9	DIFFIO_B1p	DIFFIO_B17p,DQ5B	V11	GPIO0_D23
GPIO0_D22	R10	DIFFIO_B2n	DIFFIO_B18n,DM4B	AA10	GPIO0_D9
GPIO0_D30	V5	DIFFIO_B2p	DIFFIO_B18p,DQ5B	Y10	GPIO0_D24
GPIO1_D30	V6	DIFFIO_B3n,DM3B			
GPIO1_D29	U8	DIFFIO_B3p			
GPIO0_D31	U7	DIFFIO_B4n			
GPIO1_D23	R12	DIFFIO_B4p			
GPIO1_D22	R11	DIFFIO_B5n			
		DIFFIO_B5p			
GPIO1_D31	Y3	DIFFIO_B6p,DQ3B			
GPIO0_D29	W6	DIFFIO_B7n			
GPIO0_D14	AB4	DIFFIO_B7p,DQ3B			
GPIO0_D15	AA4	DIFFIO_B8n			
		DIFFIO_B8p,DQ3B			
GPIO0_D12	AB5	DIFFIO_B9n			
GPIO0_D13	AA5	DIFFIO_B9p,DQ3B			
GPIO1_D28	Y7	DIFFIO_B10n,DQ3B			
GPIO0_D28	W7	DIFFIO_B10p,DQ3B			
GPIO1_D26	V8	DIFFIO_B11n,DQ3B			
GPIO1_D17	AB7	DIFFIO_B11p,DQ3B			
GPIO1_D16	AA7	DIFFIO_B12n,DQ5B			
		DIFFIO_B12p,DM5B			
GPIO1_D24	Y8	DIFFIO_B13p,DQ5B			
GPIO1_D25	U10	DIFFIO_B14n,DQ5B			
GPIO0_D10	AB8	DIFFIO_B14p			
GPIO0_D11	AA8	DIFFIO_B15n,DQ5B			
GPIO1_D14	AB9	DIFFIO_B15p,DQ5B			
GPIO1_D15	AA9	DIFFIO_B16n,DQS5B			
		DIFFIO_B16p,DQ5B			

BANK3

IO3_0 T11
 IO3_1 U11
 IO3_2 AB10
 IO,DQS1B Y6
 IO,DQ3B W8
 IO,DQS3B V10
 IO,VREFB3N0 V9
 IO,VREFB3N1 Y4

AB3 GPIO0_CLKOUT0
 AA3 GPIO0_CLKOUT1
 AB11 GPIO1_CLKIN0
 AA11 GPIO1_CLKIN1
 CLK14,DIFFCLK_6n
 CLK15,DIFFCLK_6p

EP3C16F484

U4D


GPIO0_D6	AB13	DIFFIO_B19n,DQ4B			
GPIO0_D7	AA13	DIFFIO_B19p,DQ4B			
GPIO0_D5	AB14	DIFFIO_B20n,DQ4B			
GPIO0_D4	AA14	DIFFIO_B20p,DQ4B			
GPIO0_D18	Y13	DIFFIO_B21n,DQS4B			
GPIO0_D19	W13	DIFFIO_B21p,DQ4B			
GPIO0_D3	AB15	DIFFIO_B22n,DQ4B			
GPIO0_D2	AA15	DIFFIO_B22p,DQ4B			
GPIO1_D21	T12	DIFFIO_B23n			
GPIO1_D20	U12	DIFFIO_B23p,DQ4B			
GPIO0_D0	AB16	DIFFIO_B24n,DQ2B			
GPIO0_D1	AA16	DIFFIO_B24p,DM2B			
GPIO1_D7	AB17	DIFFIO_B25n			
GPIO1_D6	AA17	DIFFIO_B25p			
GPIO0_D16	V14	DIFFIO_B26n,DQ2B			
GPIO0_D20	U13	DIFFIO_B26p			
GPIO1_D12	W15	DIFFIO_B27n,DQ2B			
GPIO1_D13	V15	DIFFIO_B27p,DQ2B			
GPIO1_D11	T15	DIFFIO_B28n,DQ2B			
GPIO1_D18	T14	DIFFIO_B28p			
GPIO1_D8	Y17	DIFFIO_B29n,DQS0B			
GPIO1_D9	W17	DIFFIO_B29p,DQ2B			
GPIO1_D1	AB20	DIFFIO_B30n,DQ2B			
GPIO1_D0	AA20	DIFFIO_B30p			
GPIO0_D17	U14	DIFFIO_B31n			
GPIO1_D10	U15	DIFFIO_B31p			
		DIFFIO_B32n			
GPIO1_D19	R14	DIFFIO_B32p			

BANK4

IO4_0 R13
 IO4_1 V12
 IO4_2 AA18
 IO,DQ2B AB18
 IO,DQS2B V13
 IO,RDN2 AB19
 IO,RUP2 AA19
 IO,VREFB4N0 V16
 IO,VREFB4N1 W14

R16 GPIO1_CLKOUT0
 T16 GPIO1_CLKOUT1
 AB12 GPIO0_CLKIN0
 AA12 GPIO0_CLKIN1
 CLK12,DIFFCLK_7n
 CLK13,DIFFCLK_7p

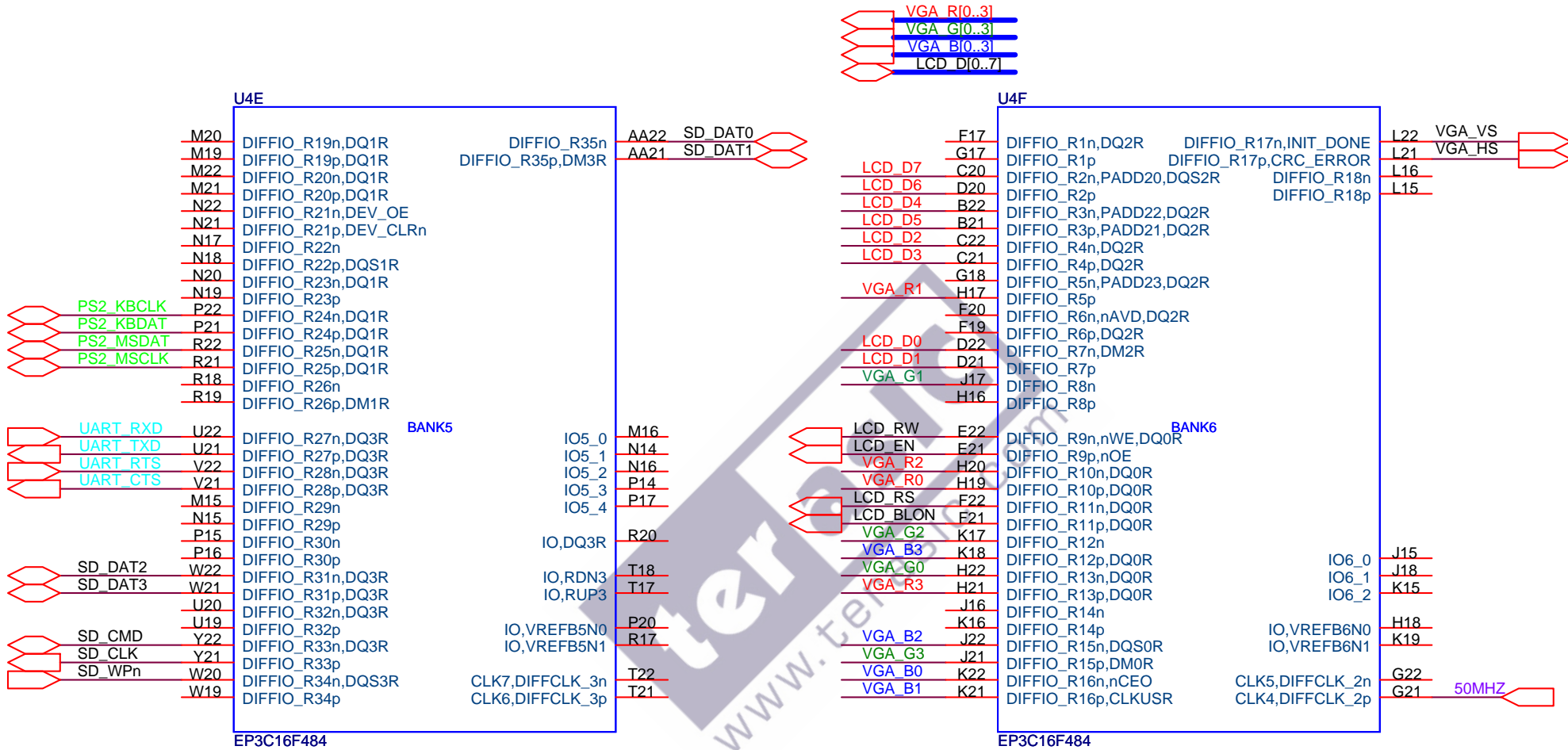
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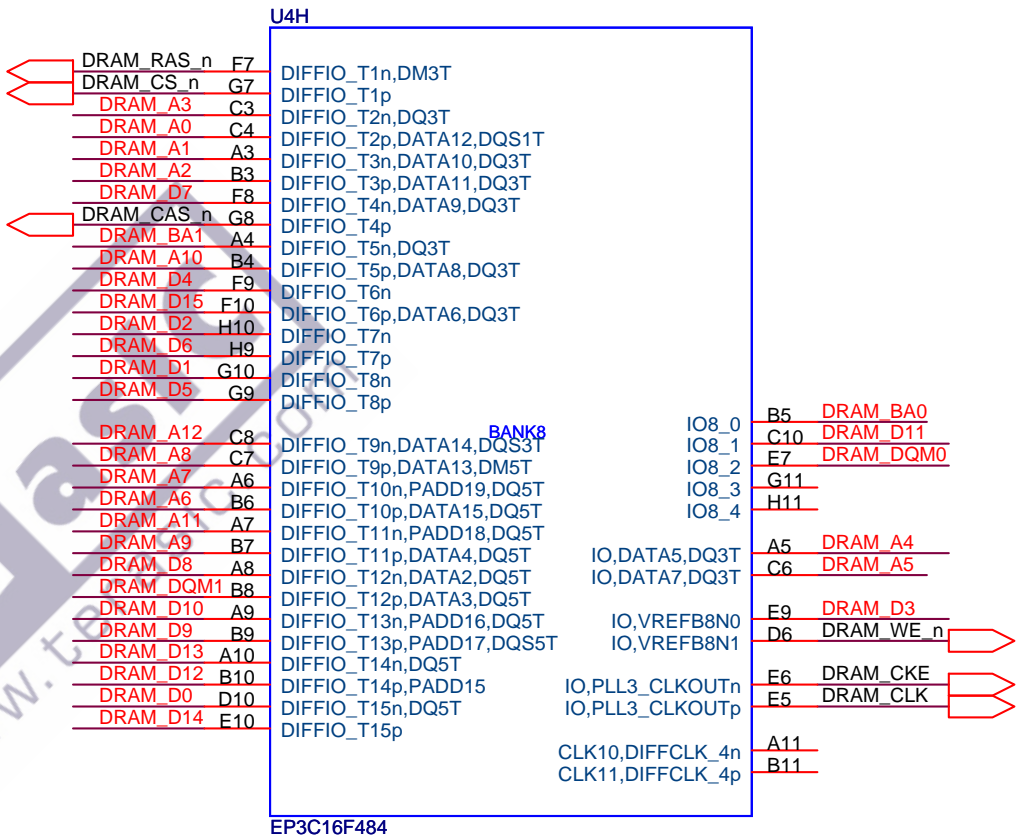
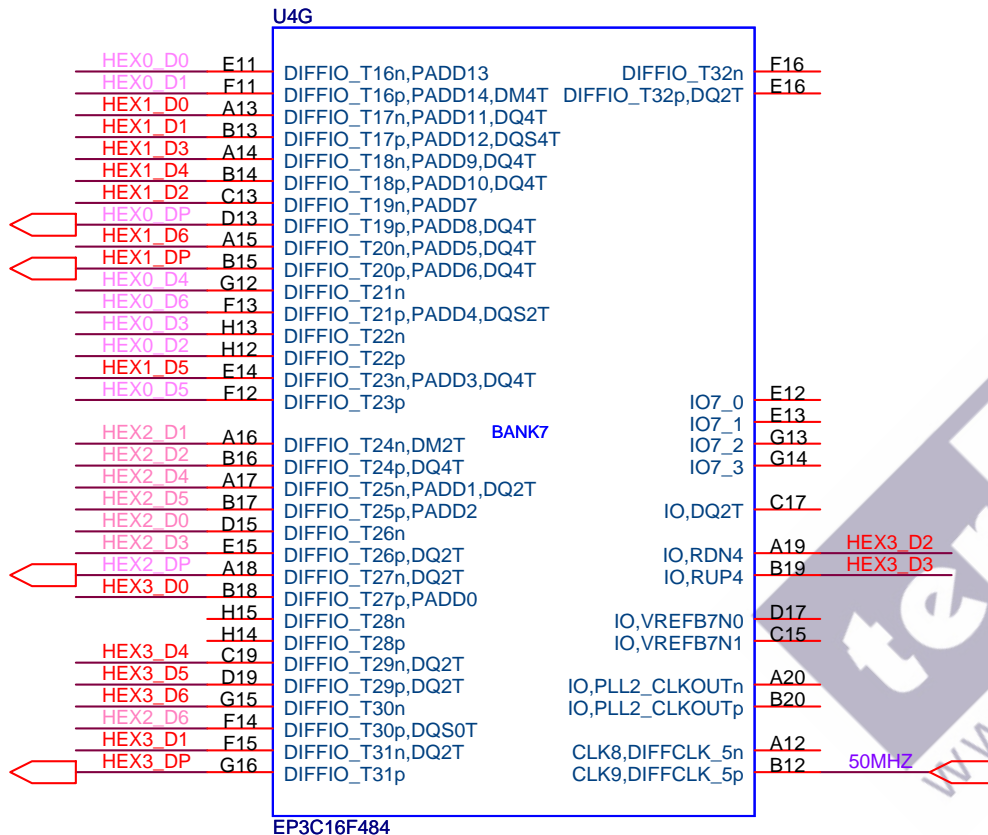
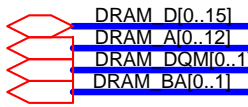
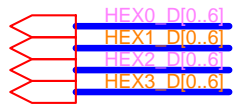

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Title
 ALTERA DE0

Size A	Document Number BANK3, BANK4	Rev 1.1
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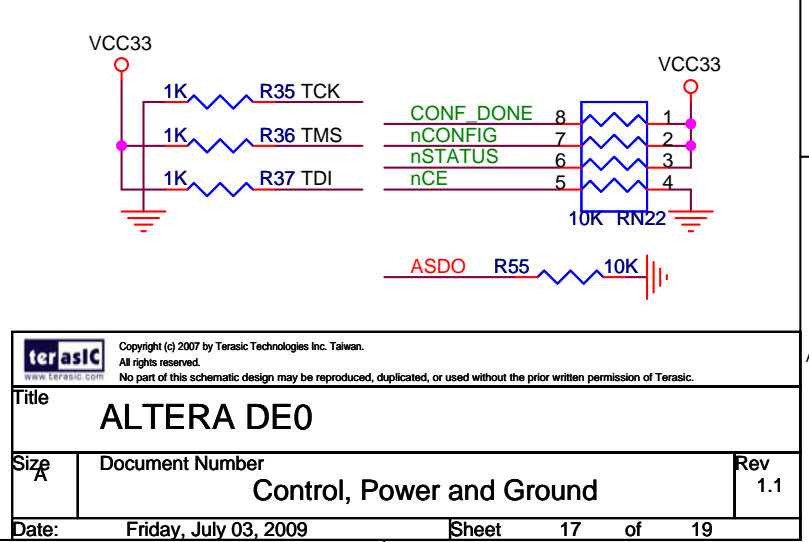
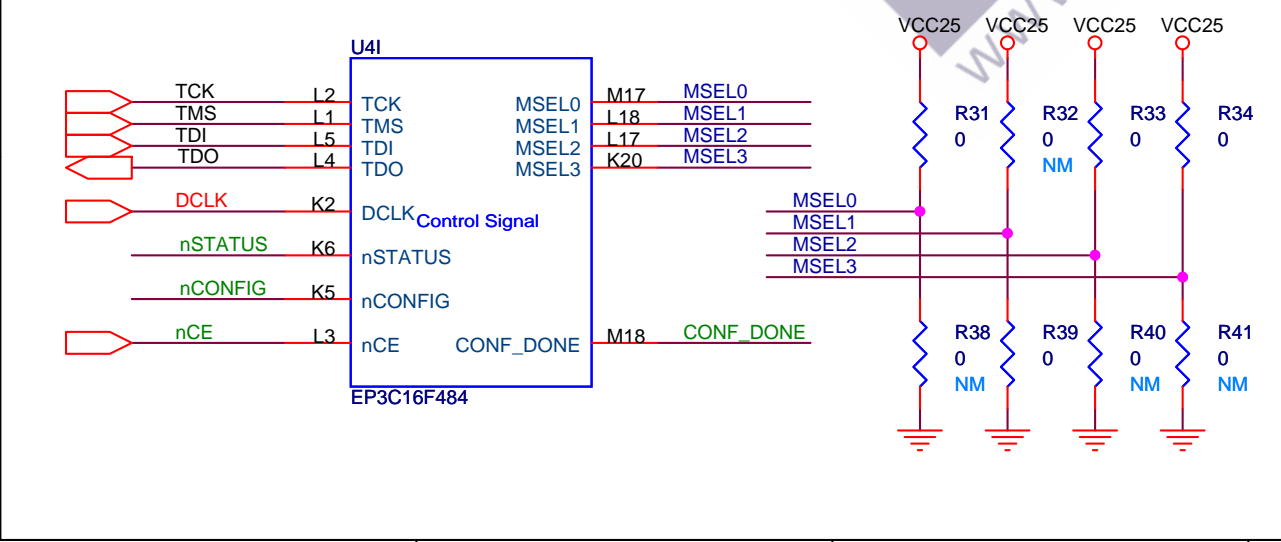
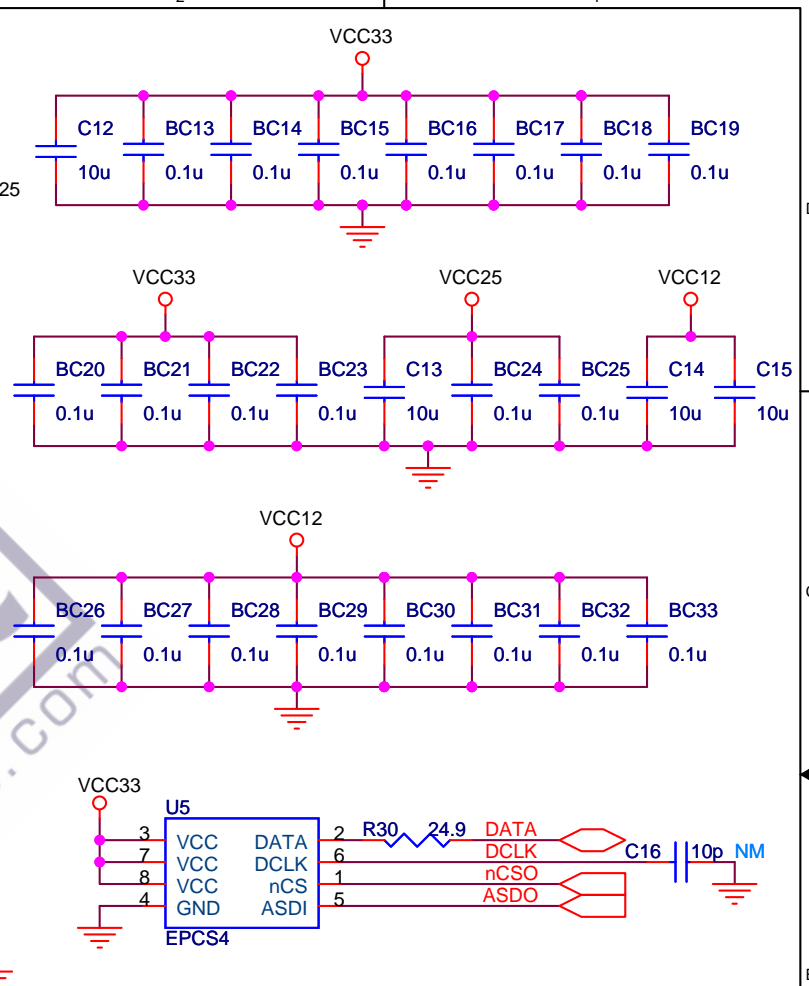
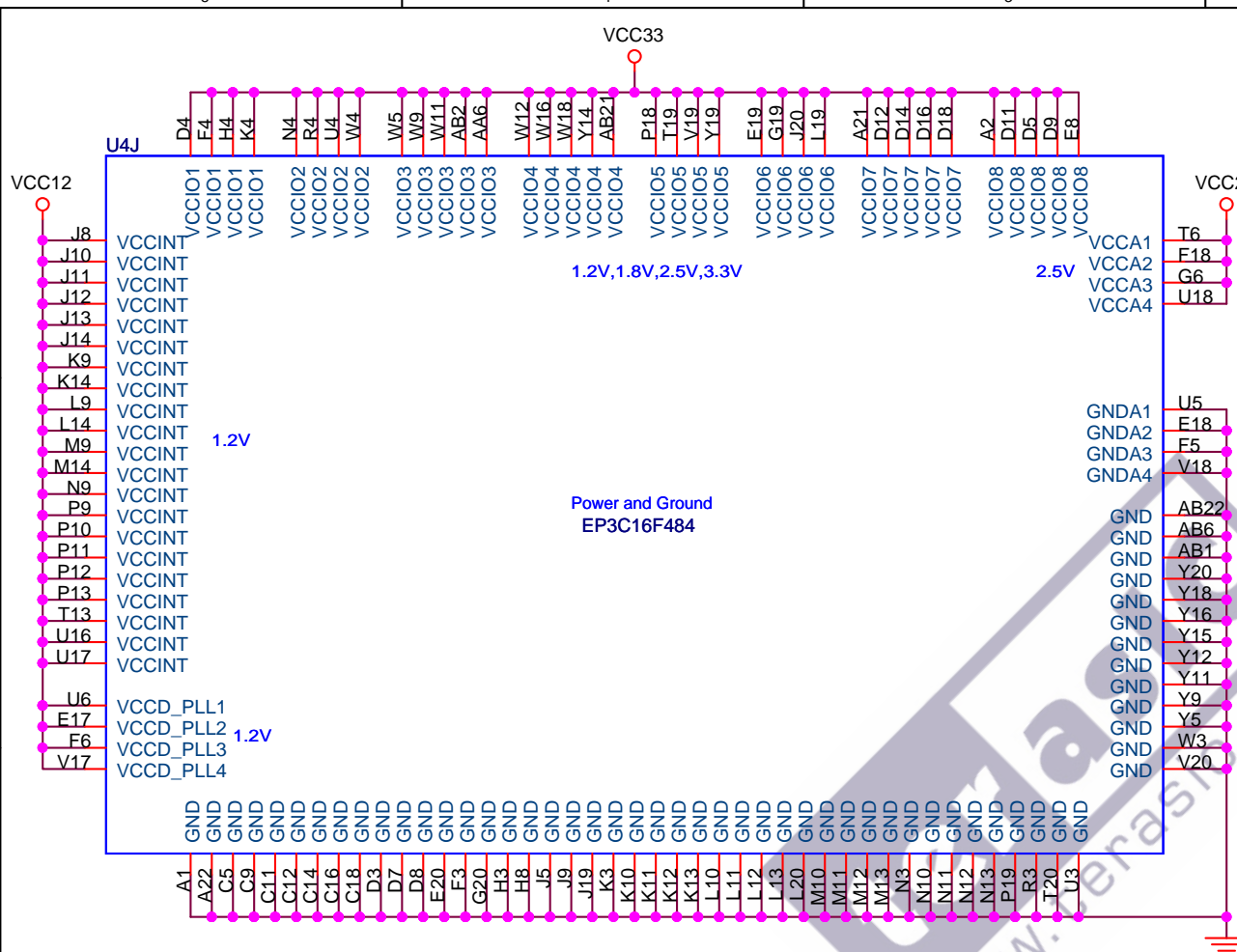


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Title: **ALTERA DE0**

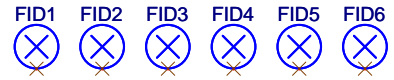
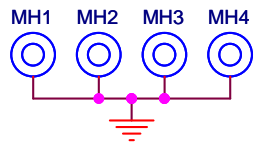
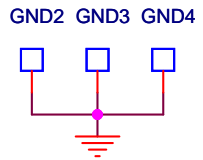
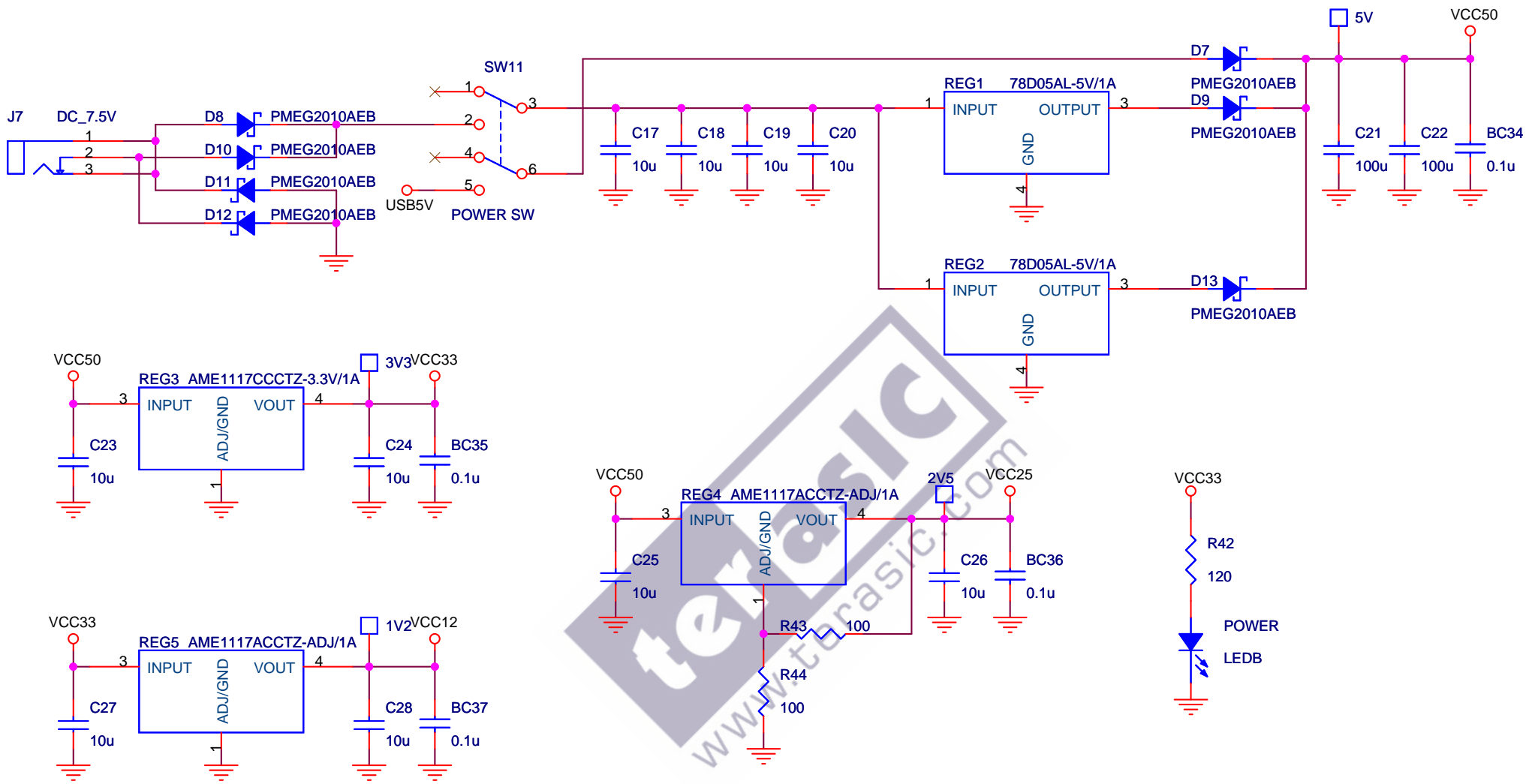
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Title		
ALTEA DE0		
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A	Control, Power and Ground	1.1
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Title		
ALTERA DE0		
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A	POWER	1.1
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